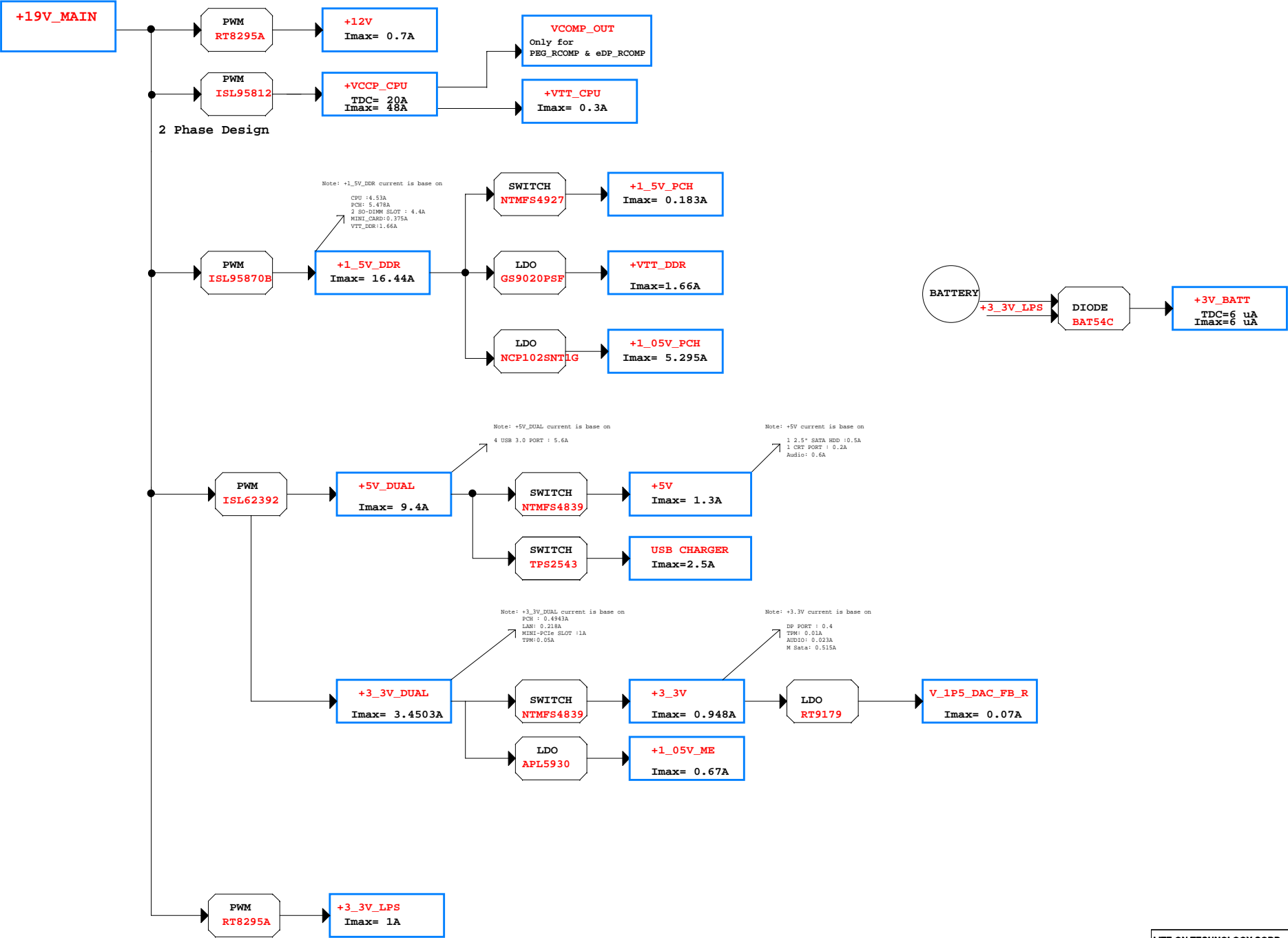


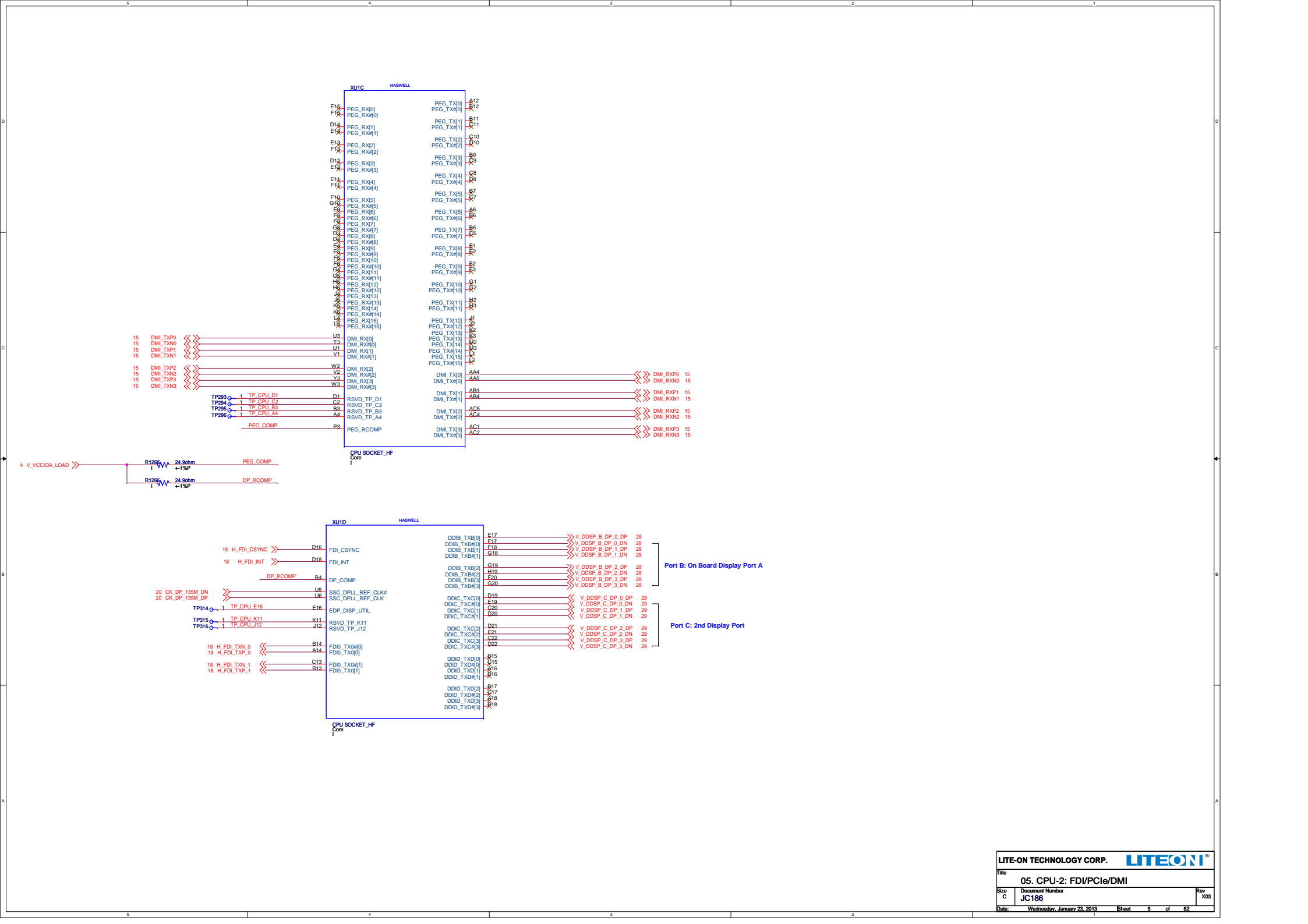
PAGE	TITLE
01	Block Diagram
02	Power Sequence
03	Power Delivery Map
04	CPU-1: MSIC
05	CPU-2: FDI/PCIe/DMI
06	CPU-3: DDR3 CHA
07	CPU-4: DDR3 CHB
08	CPU-5: Power
09	CPU-6: GND
10	DDR3 CHA SO-DIMM1
11	Blank
12	DDR3 CHB SO-DIMM3
13	Blank
14	PCH-1: PCI
15	PCH-2: DMI/PCIe/USB
16	PCH-3: SATA/HOST/FAN
17	PCH-4: LPC/HDA/RTC/SMB/SPI
18	PCH-5/7: NVRAM/FDI
19	PCH-6: Display
20	PCH-8: Clock
21	PCH-9: Power 1
22	PCH-10: Power 2
23	PCH-11: GND
24	PCH Misc conn/Buz/ID
25	DSW
26	SPI/ XDP
27	Asset ID - PCA24S08AD
28	Display Port B
29	Display Port C
30	Audio Codec - ALC283-CG
31	LAN - Intel CLARKVILLE-LM
32	TPM - ST ST33ZP24AR28PVSH
33	SIO IT8733F
34	USB3.0 ODD CONN / Int USB
35	USB3.0 CONN x 3
36	USB3.0 x1/ USB CHARGER
37	Mini PCIE/ 2 COM PORT
38	MSATA
39	FAN CTRL
40	Buzzer/Parallel Port/BATT
41	SATA HDD
42	VGA
43	PWRGD & Bleed Off
44	Button/LED
45	SM BUS/Thermal Sensing/APS
46	Debug Port
47	Mounting Hole
48	Blank
49	DC +19V MAIN / POWER METER
50	+5V_DUAL / +3_3V_DUAL
51	+5V/ +3.3V/ +3_3V_LPS/ ME
52	+12V
53	VCORE CONTROLLER
54	VCORE OUTPUT
55	+1.5V_DDR / +VTT_DDR
56	+1.5_PCH / +1_05PCH
57	+1_05V_ME / +5V_USB
58	STRAPPING PIN
59	PCH GPIO TABLE
60	SIO GPIO TABLE
61	Change List
62	Change List2



POWER CONN



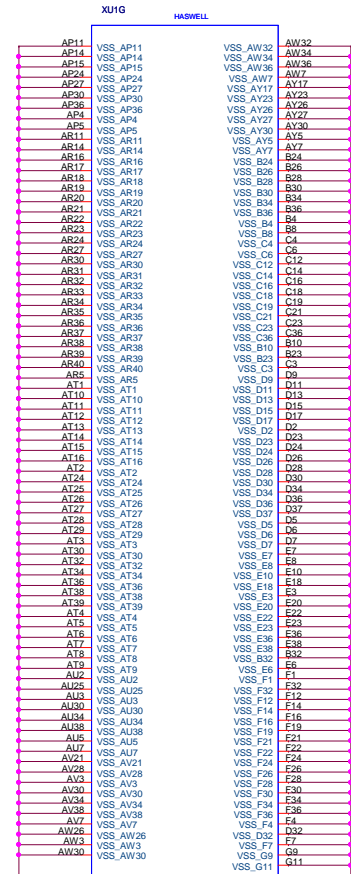




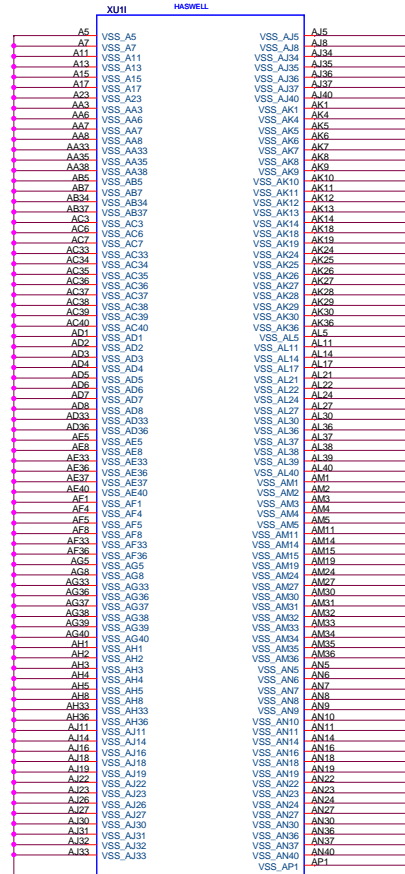




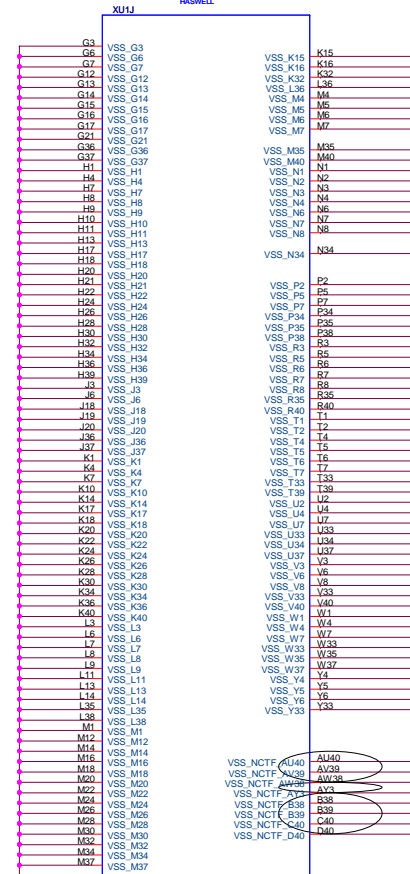




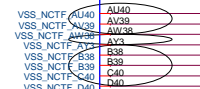
CPU SOCKET\_HF  
Core



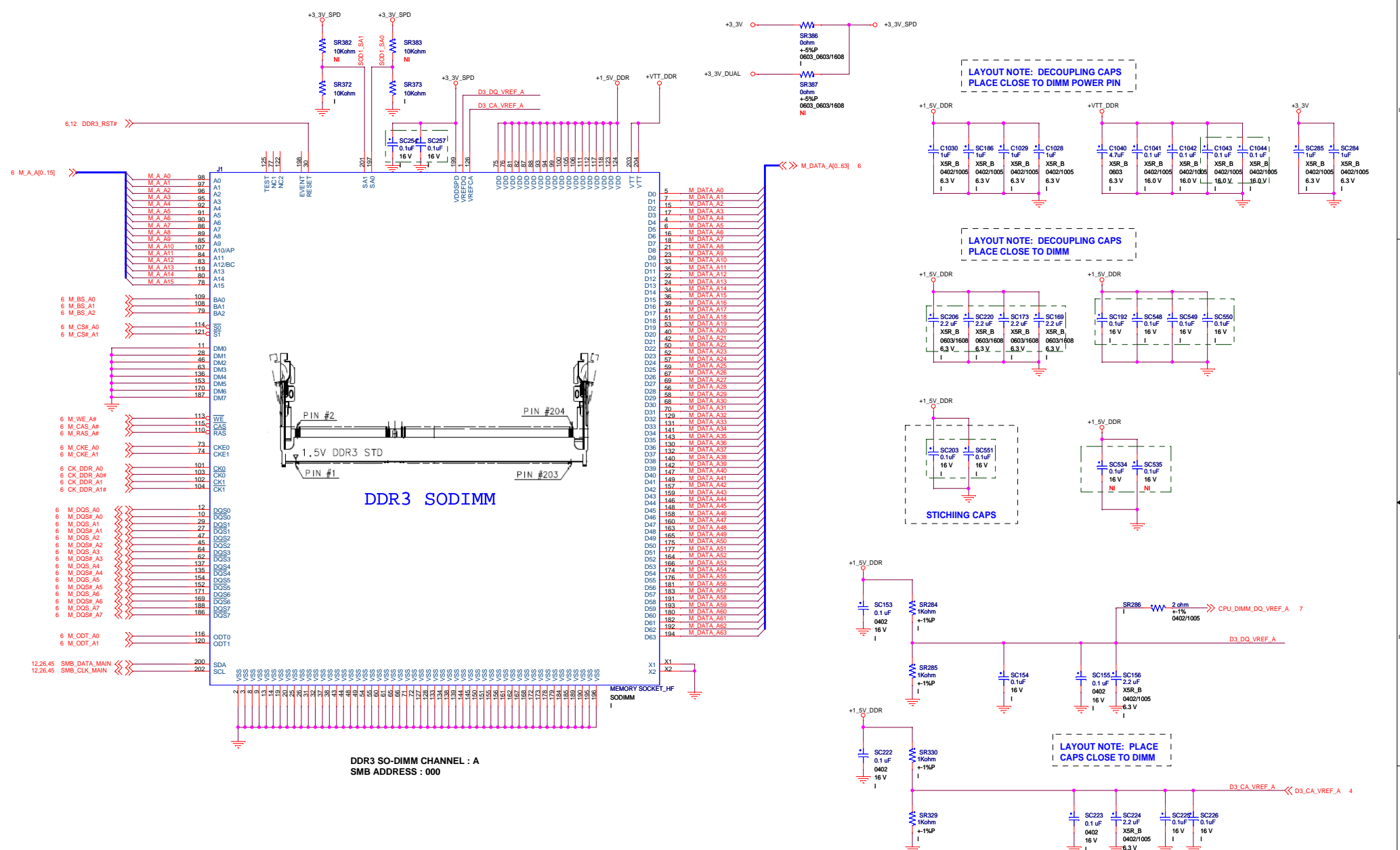
CPU SOCKET\_HF  
Core



CPU SOCKET\_HF  
Core

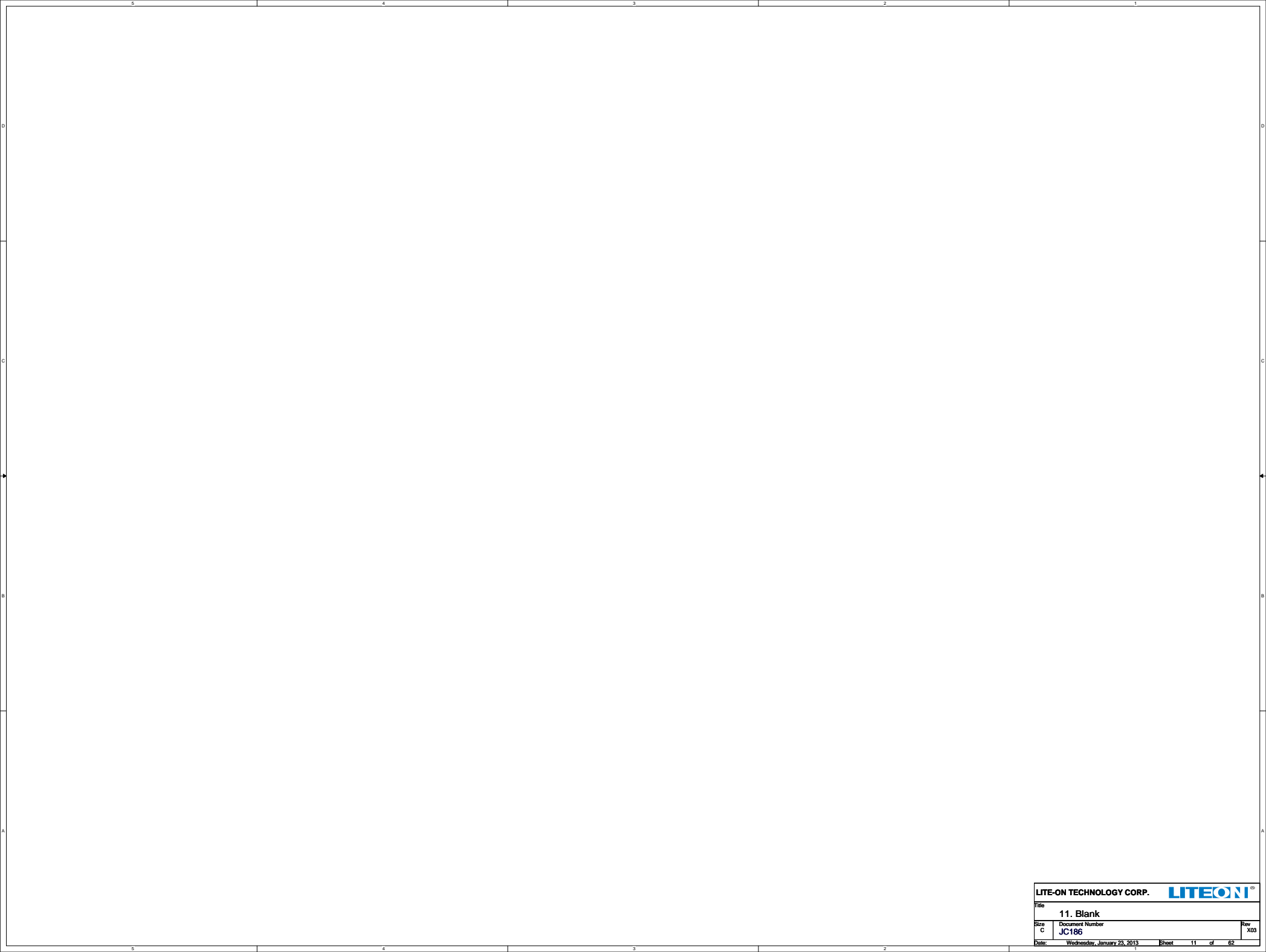



Left down Pin of CPU  
Up Left Pin of CPU  
Right down Pin of CPU

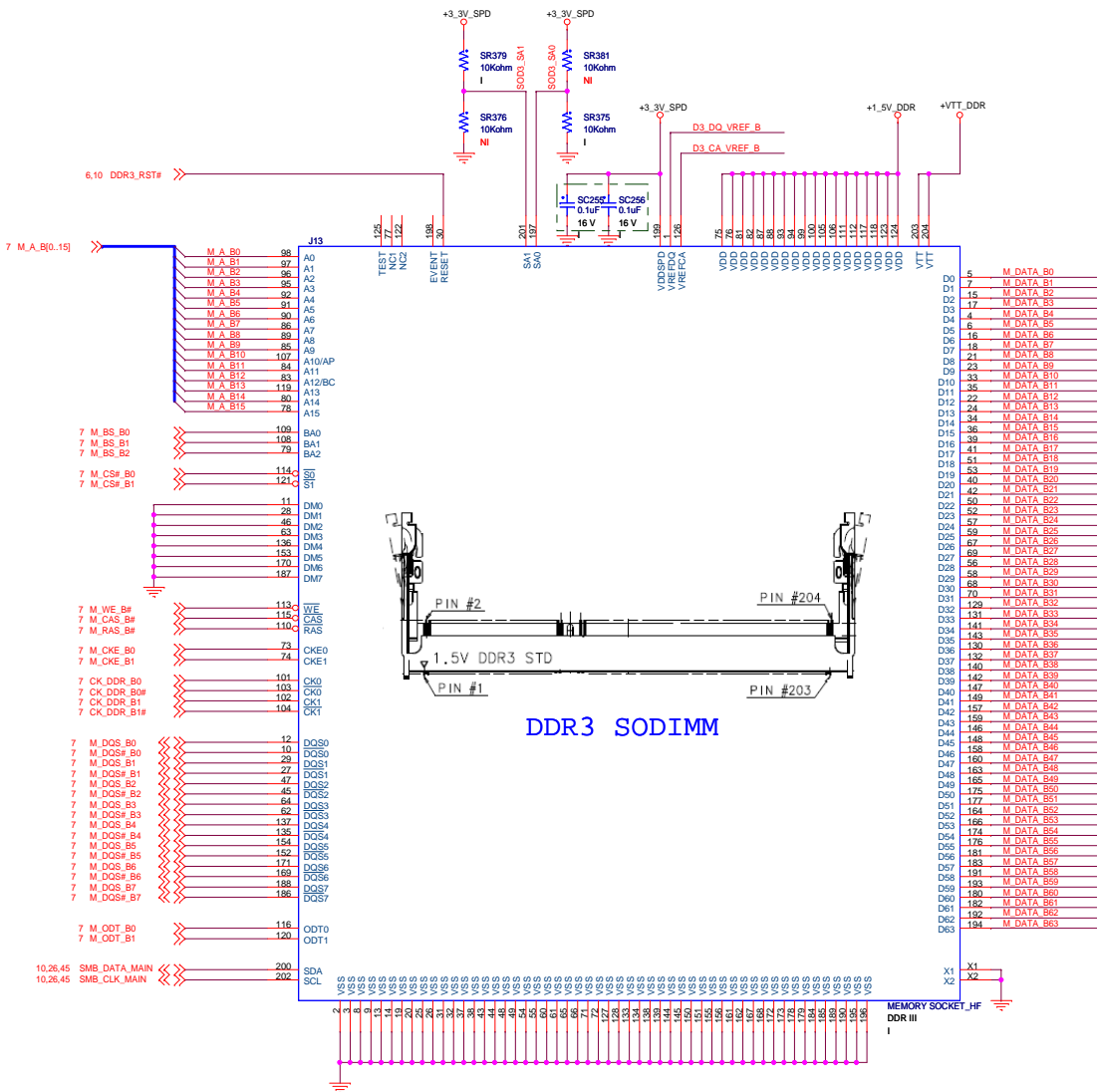


DDR3 SODIMM

DDR3 SO-DIMM CHANNEL : A  
SMB ADDRESS : 000

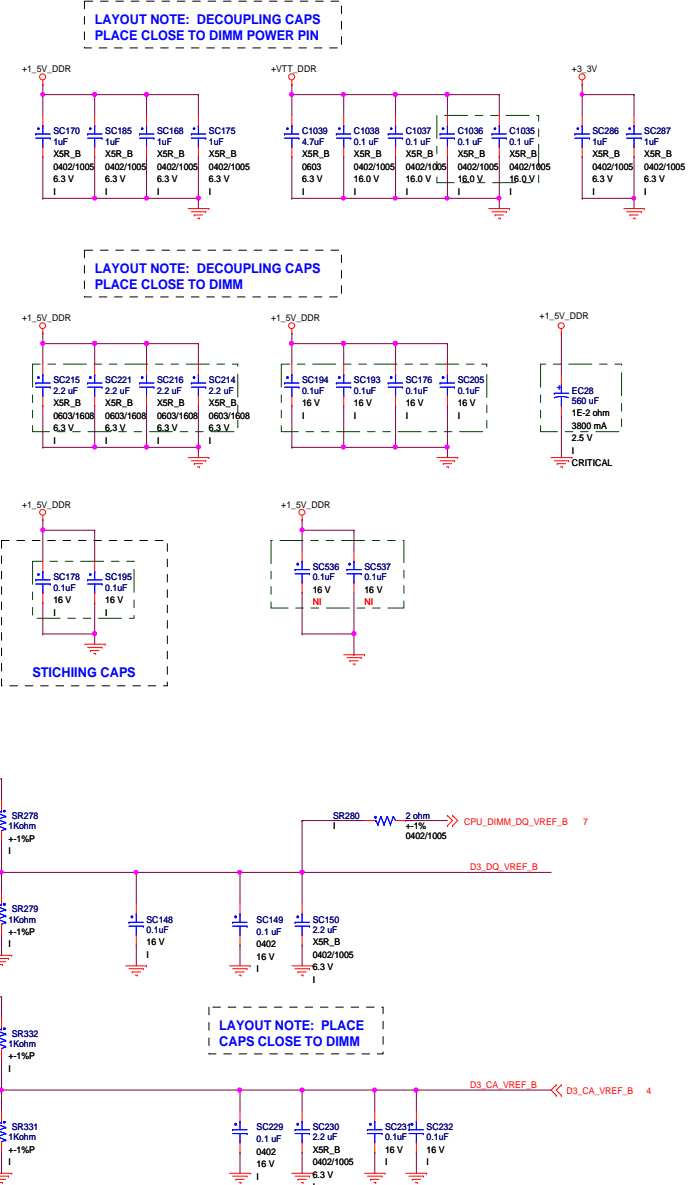


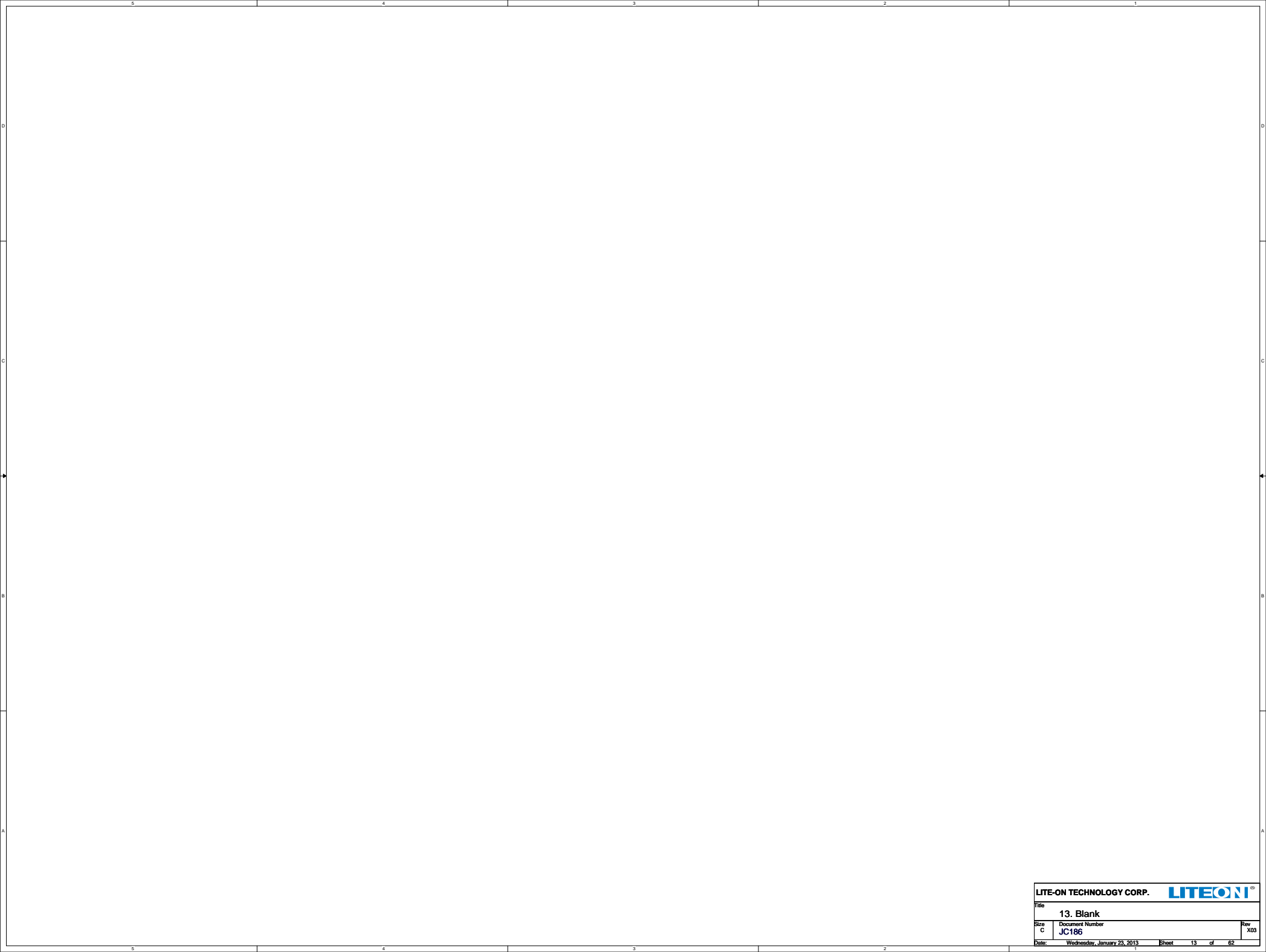
LITE-ON TECHNOLOGY CORP.			
Title			
11. Blank			
Size	Document Number	Rev	
C	JC186	X03	
Date:	Wednesday, January 23, 2013	Sheet	11 of 62




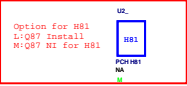
DDR3 SODIMM

DDR3 DO-DIMM CHANNEL : B  
SMB ADDRESS:010

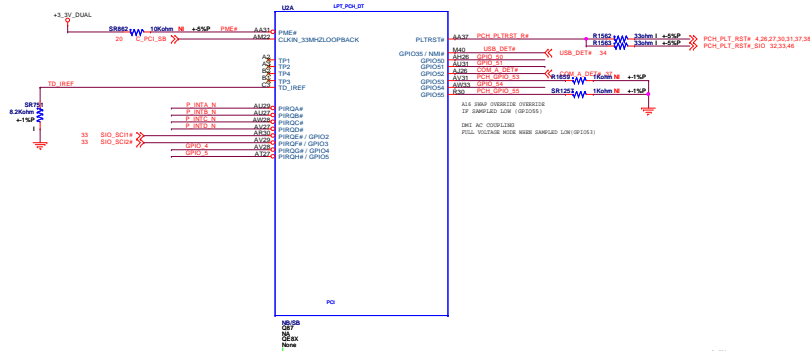




LITE-ON TECHNOLOGY CORP.			
Title			
13. Blank			
Size	Document Number	Rev	
C	JC186	X03	
Date:	Wednesday, January 23, 2013	Sheet	13 of 62

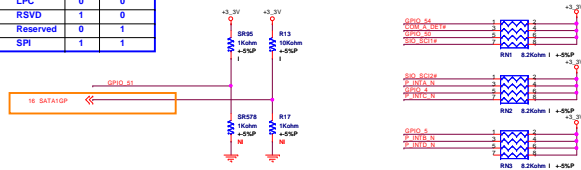


## No PCI Device



## Boot BIOS Select

Boot Device	GPIO51	SATA1GP
LPC	0	0
RSVD	1	0
Reserved	0	1
SPI	1	1



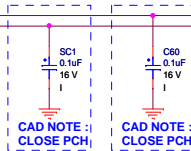








28 DDPB\_HPD\_PD  
29 DDPC\_HPD\_PD\_PCH



28 V\_DDSP\_B\_AUX\_DN  
28 V\_DDSP\_B\_AUX\_DP  
29 V\_DDSP\_C\_AUX\_DN  
29 V\_DDSP\_C\_AUX\_DP

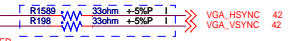
TP365  
TP366

UZE UPT\_PCH\_BT

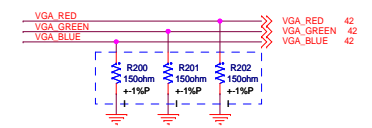
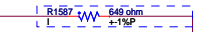
DDPB\_HPD PD AJ2  
DDPC\_HPD PD\_PCH AH5  
DDPD\_HPD PD AH4  
DDPB\_AUXN AK6  
DDPB\_AUXP AK8  
DDPC\_AUXN AG7  
DDPC\_AUXP AG8  
VDDSP\_D\_AUX\_DN AG11  
VDDSP\_D\_AUX\_DP AG10

VGA\_HSYNC AH3  
VGA\_VSYNC AH2  
VGA\_RED AC2  
VGA\_GREEN AE2  
VGA\_BLUE AC3  
VGA\_IRTN AG4  
VGA\_DDC\_DATA AL3  
VGA\_DDC\_CLK AL2  
DAC\_REF AF5  
DDPC\_CTRLCLK AN3  
DDPC\_CTRLDATA AM2  
DDPB\_CTRLCLK AM1  
DDPB\_CTRLDATA AJ5  
PCH\_DDPD\_CTRLCLK\_TP AN4  
VDDPD\_CTRLDATA AN2

CAD NOTE : CLOSE PCH within 750mils



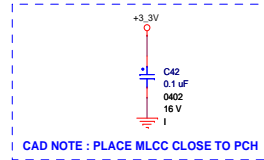
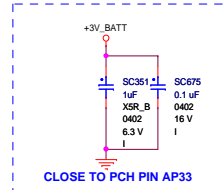
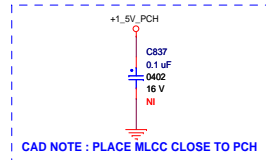
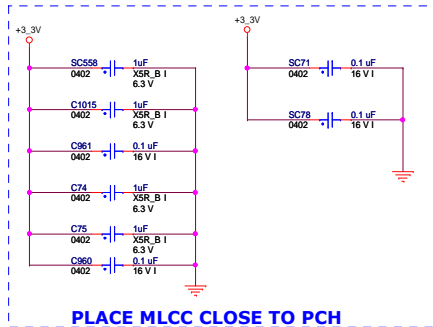
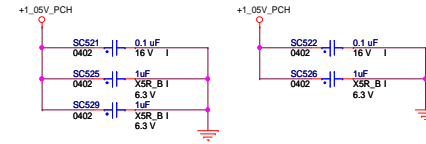
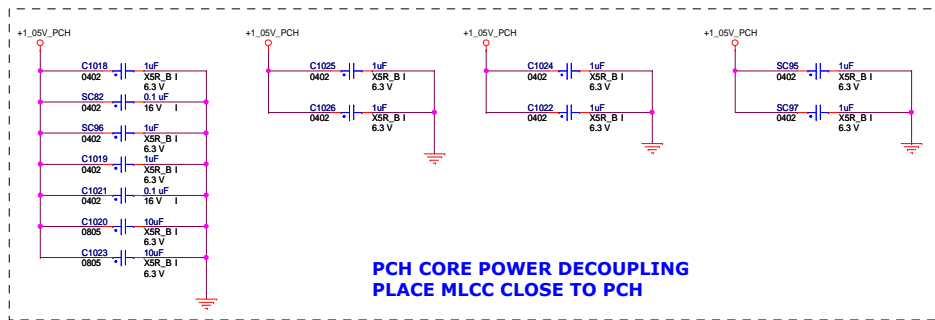
CAD NOTE : CLOSE PCH within 500mils

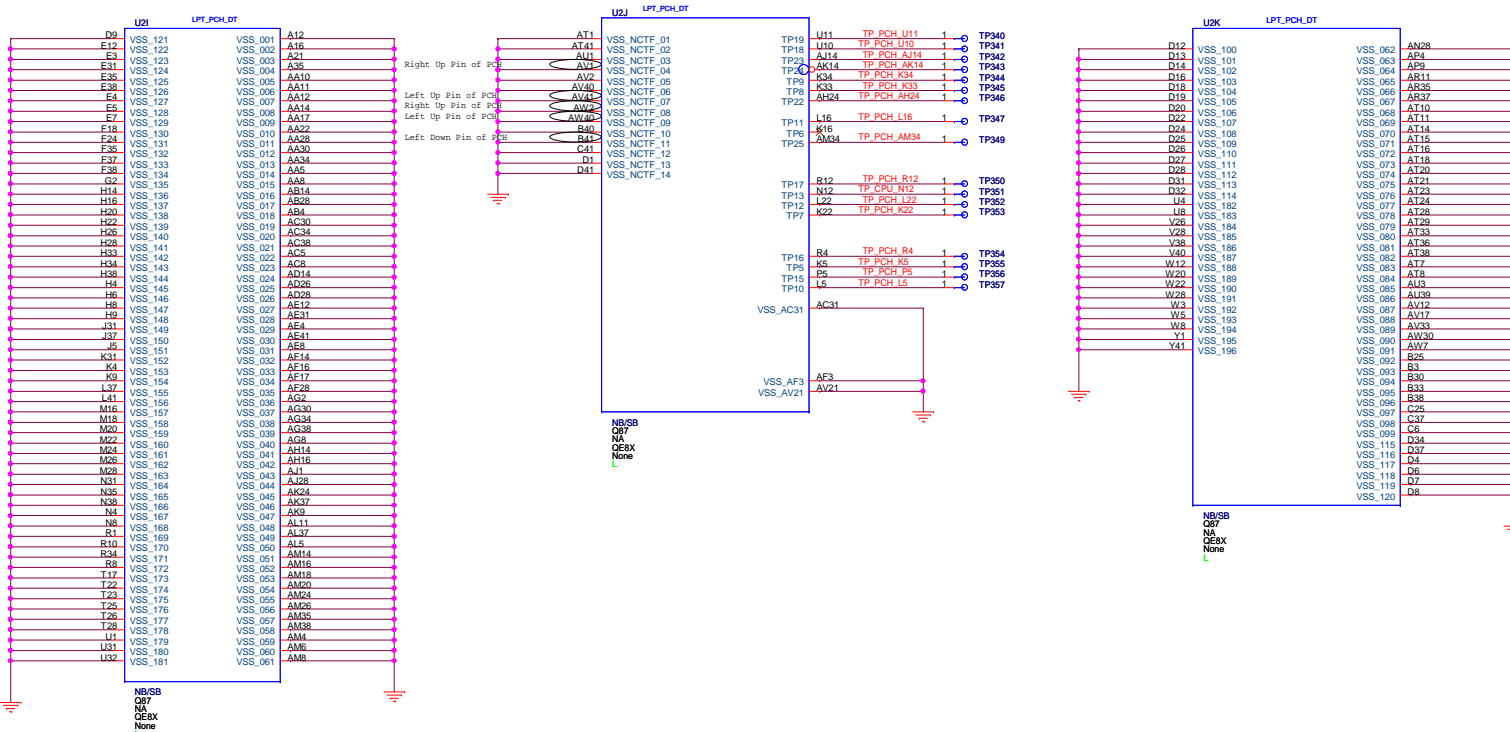


CAD NOTE : CLOSE PCH within 250mils



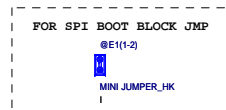
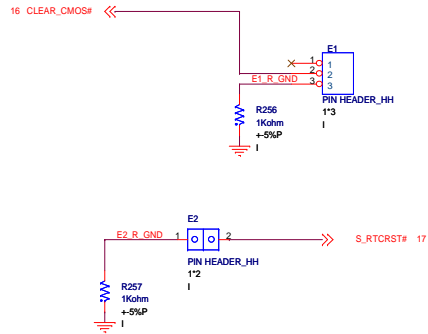








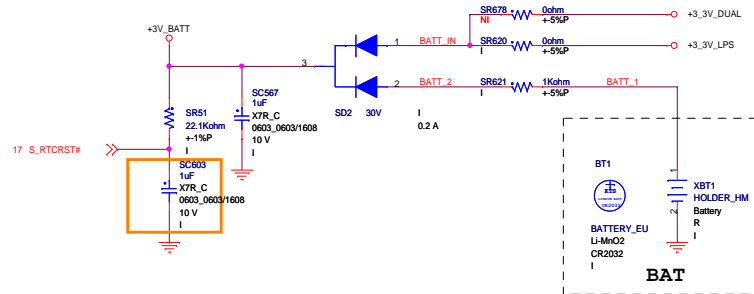
## CLEAR CMOS



Jumper	Type
Dummy	Default
Pop	CLR_CMOS

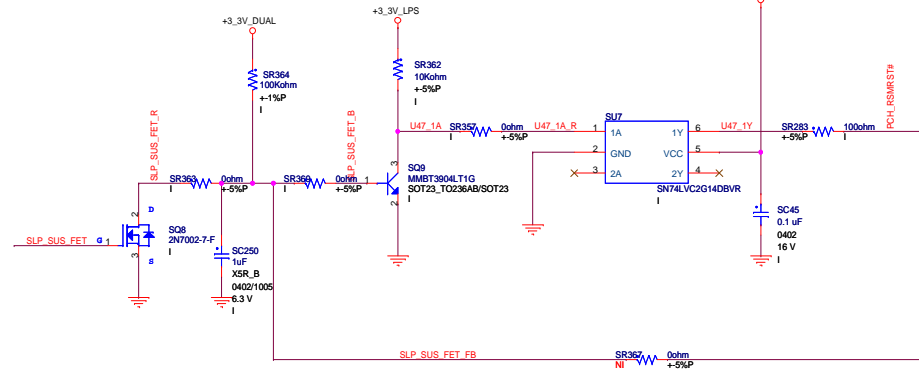
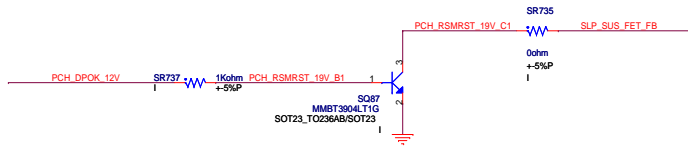
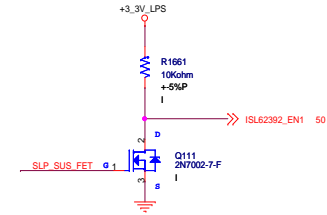
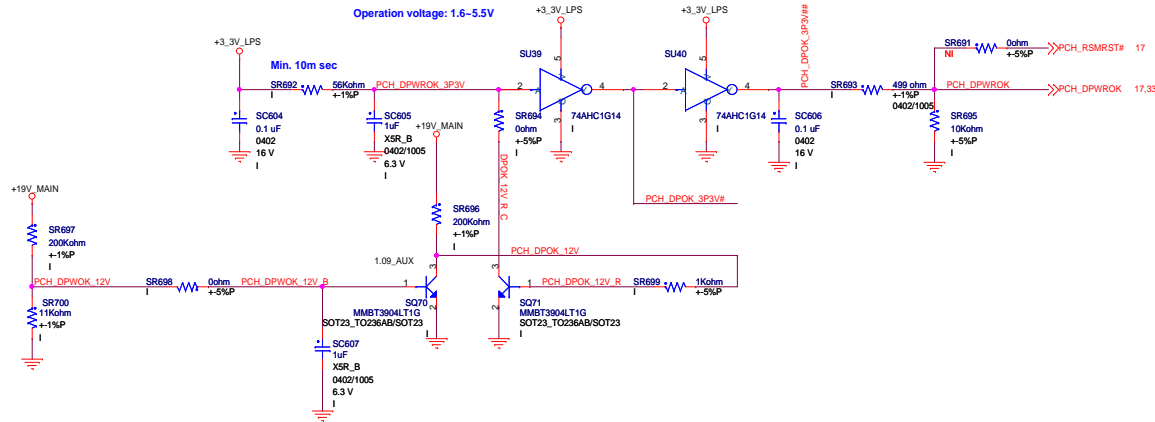


## BATTERY CIRCUIT

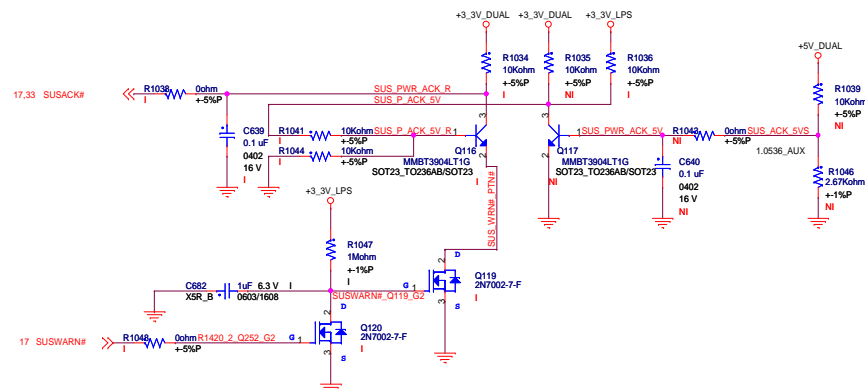


## PCH DPWROK

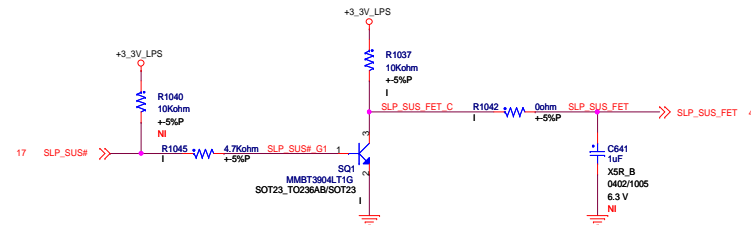
Operation voltage: 1.6~5.5V



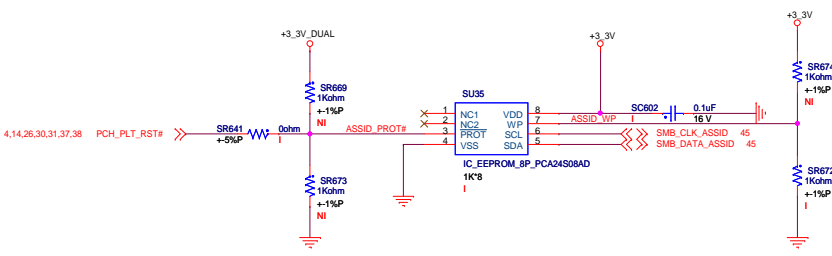
## +5V DUAL SUS ACK



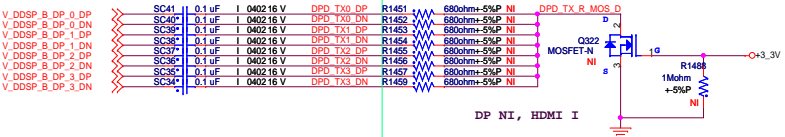
## DSW CONTROL SIGNAL





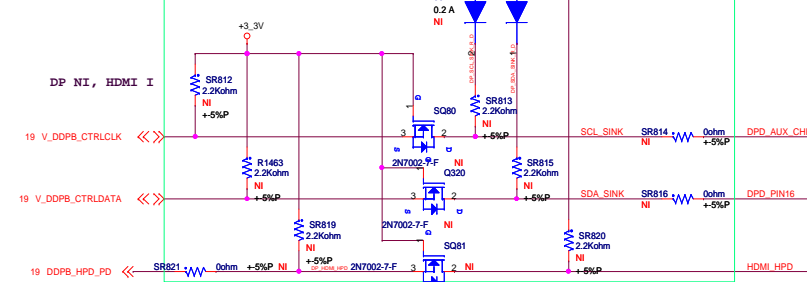


## HDMI high speed signal level shift

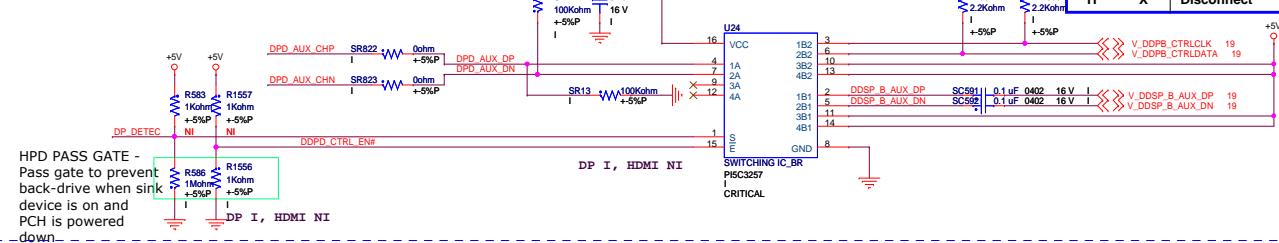


CAD Note : Please place 680 ohm component as short as passable (to bridge the antenna effect)

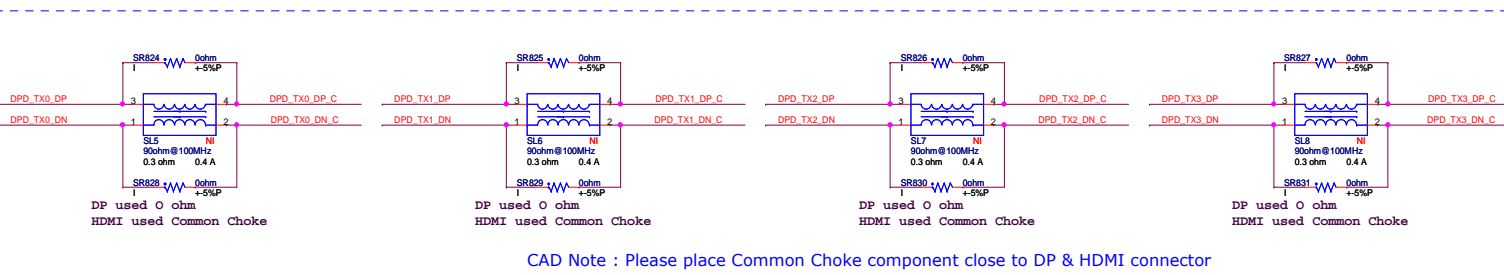
## HDMI other signal level shift



## Aux Channel Control



CAD Note : Please place ESD component close to DP connector

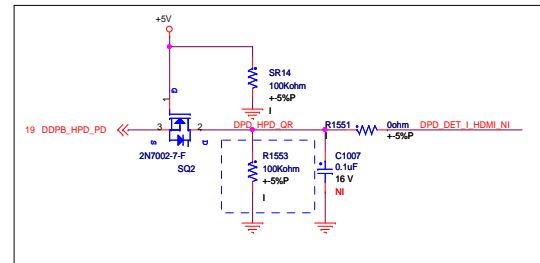
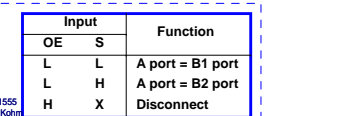


CAD Note : Please place Common Choke component close to DP & HDMI connector

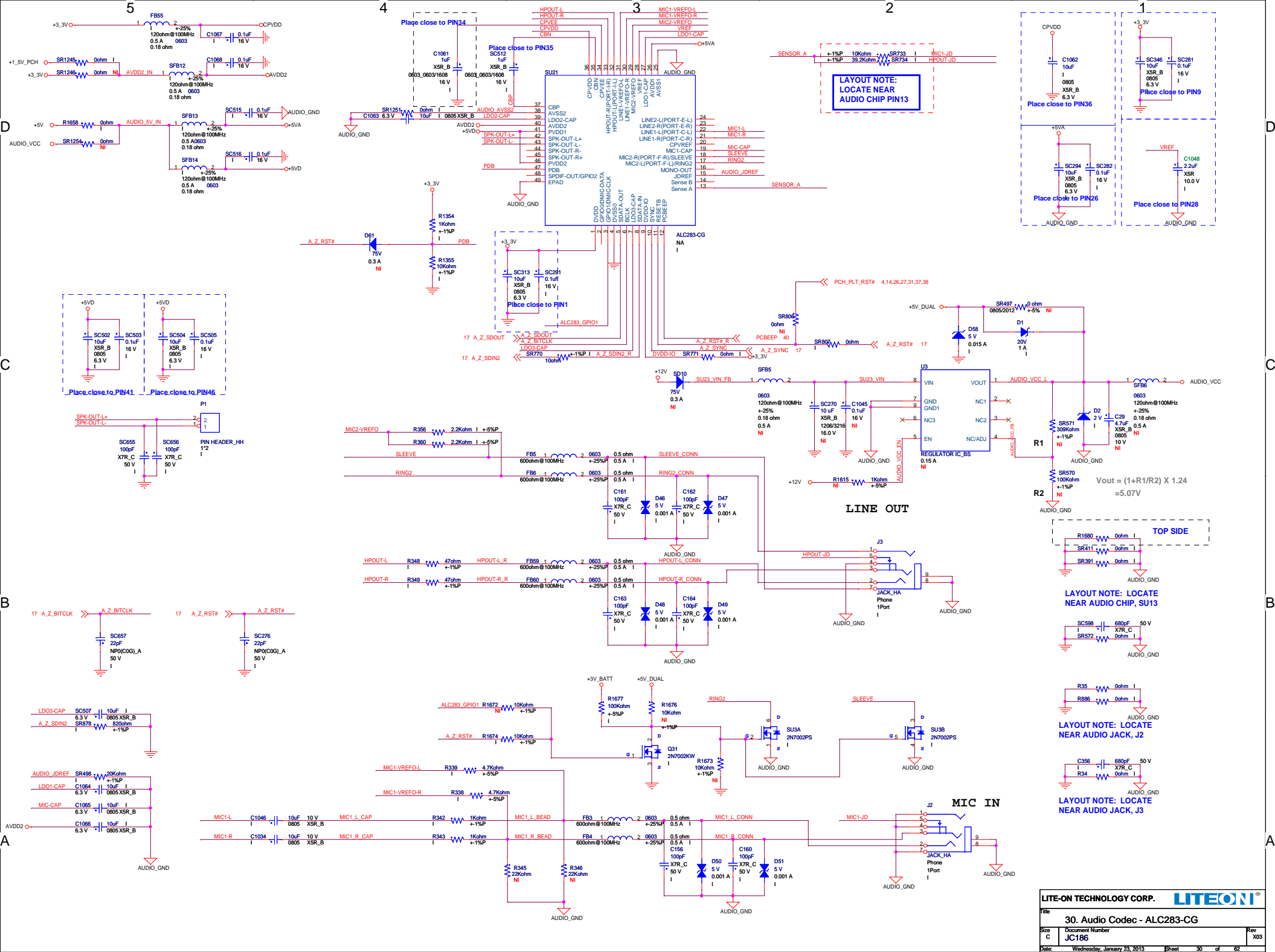
## DP & HDMI co-lay Connector

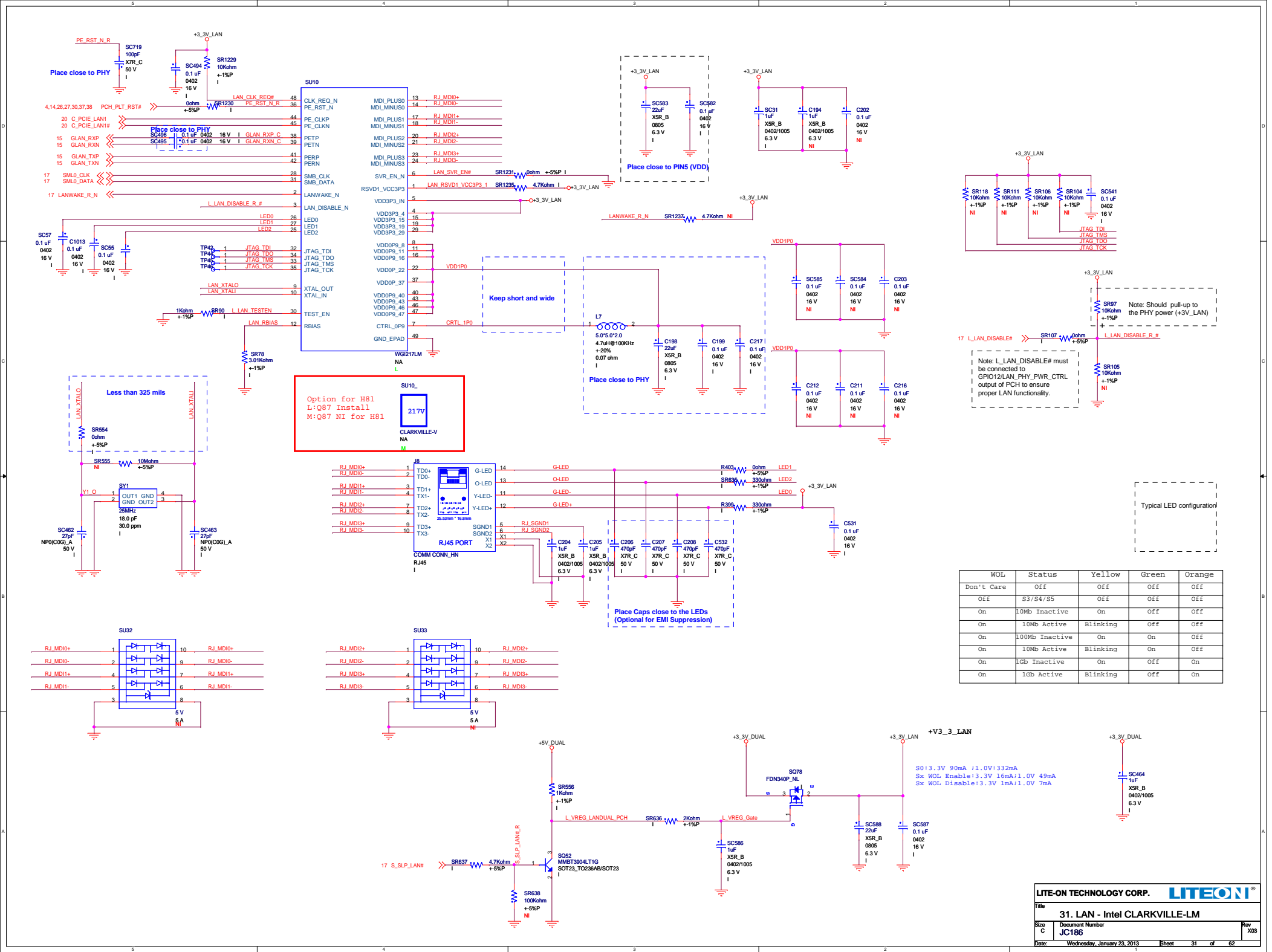


## DisplayPort Interoperability





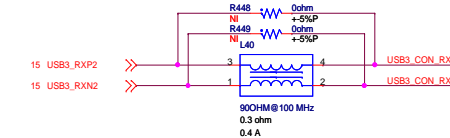
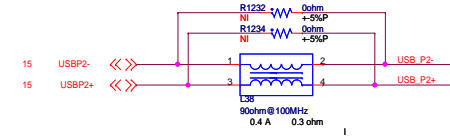
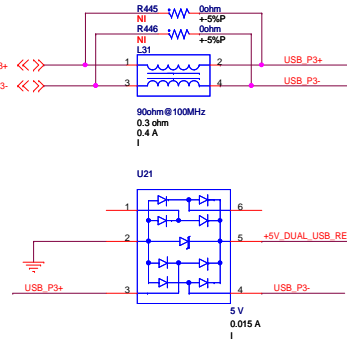
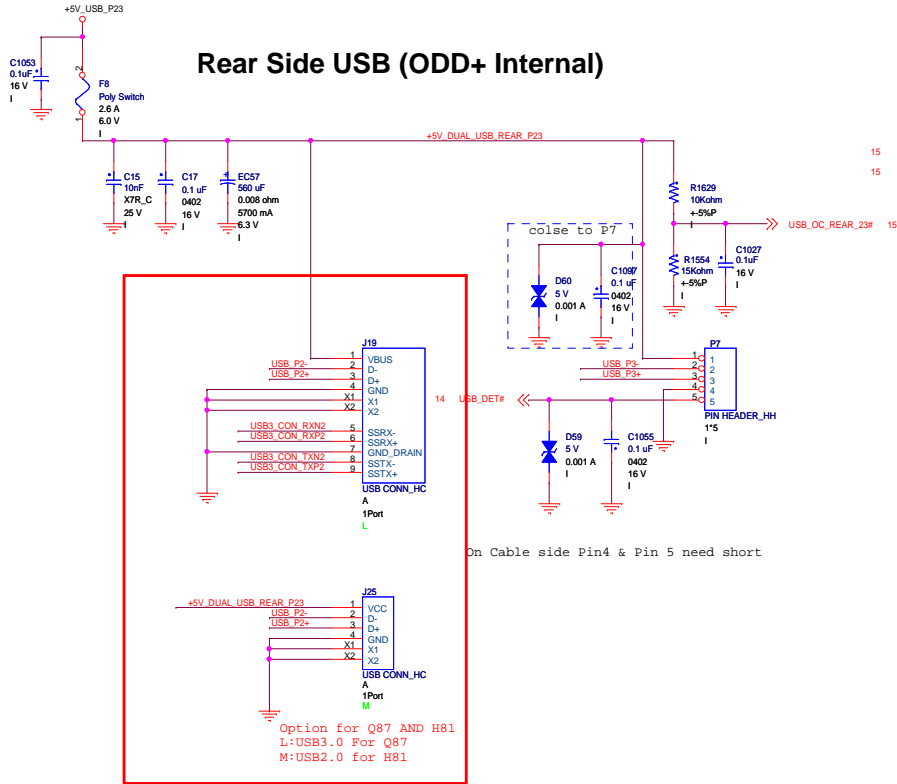




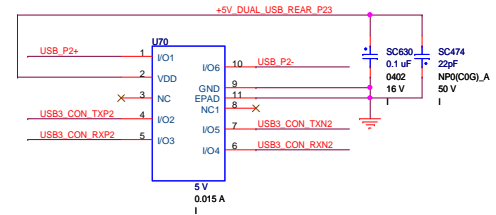
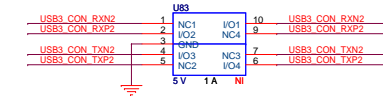
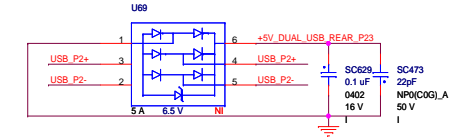
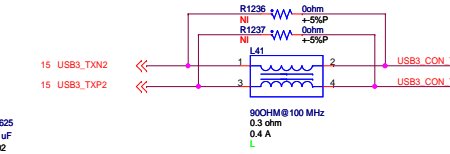




## Rear Side USB (ODD+ Internal)

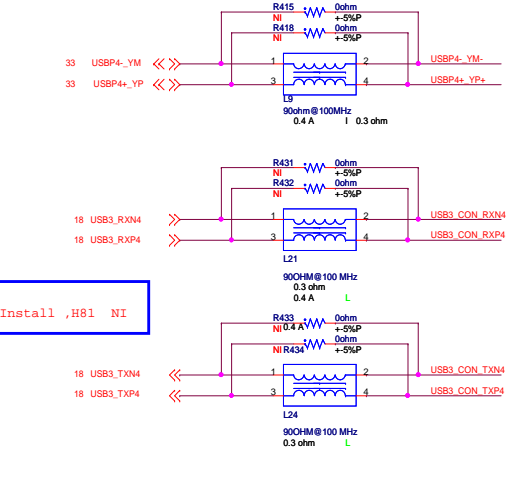
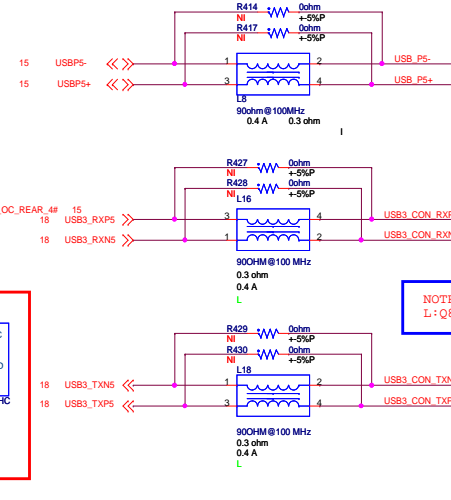
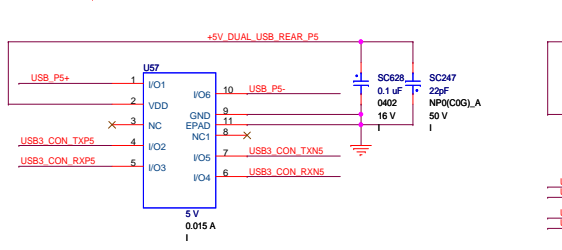
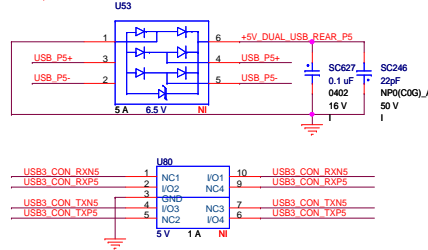
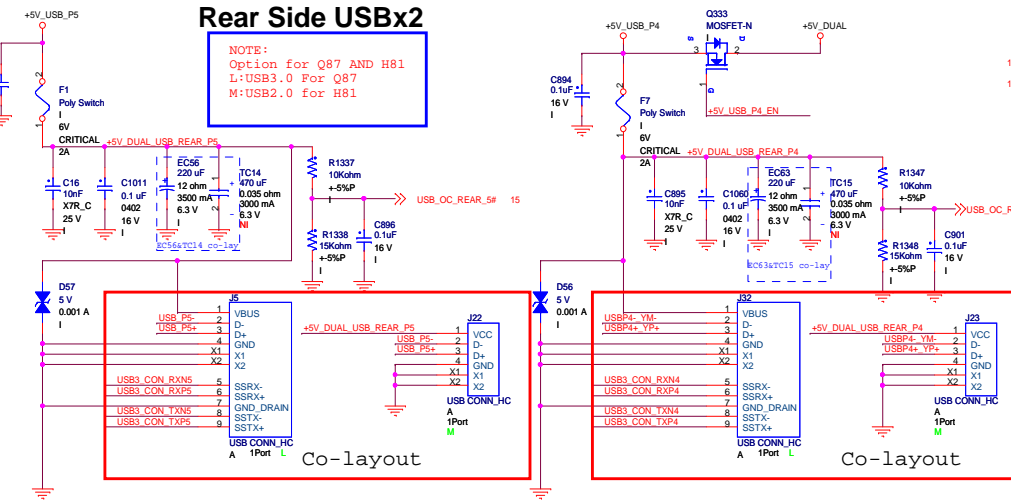


NOTE:  
L:Q87 Install ,H81 NI

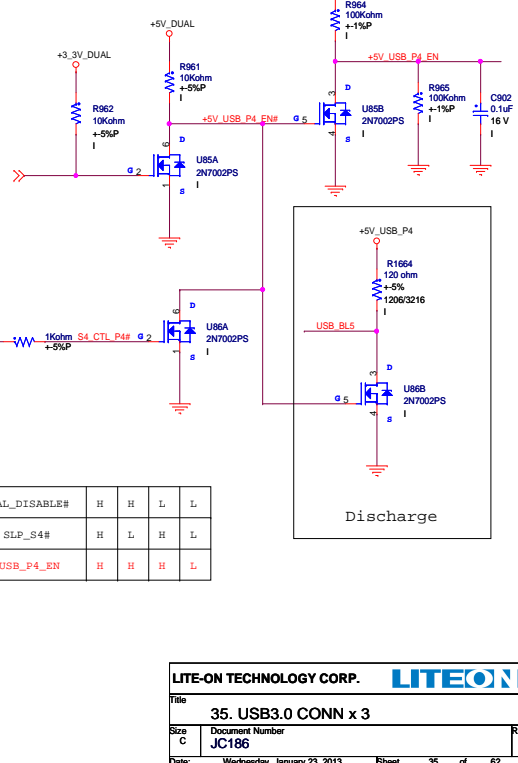
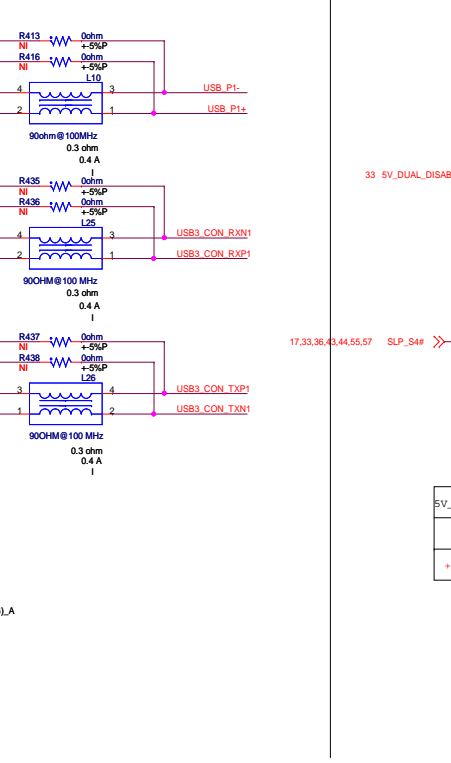
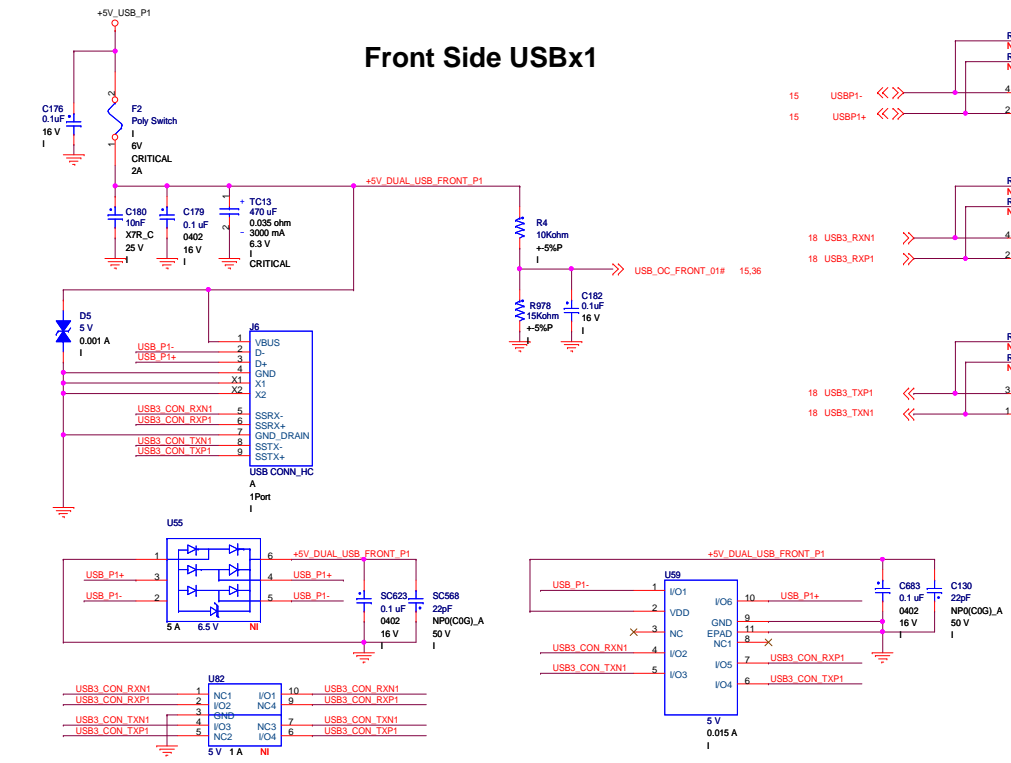


## Rear Side USBx2

NOTE:  
Option for Q87 AND H81  
L:USB3.0 For Q87  
M:USB2.0 for H81



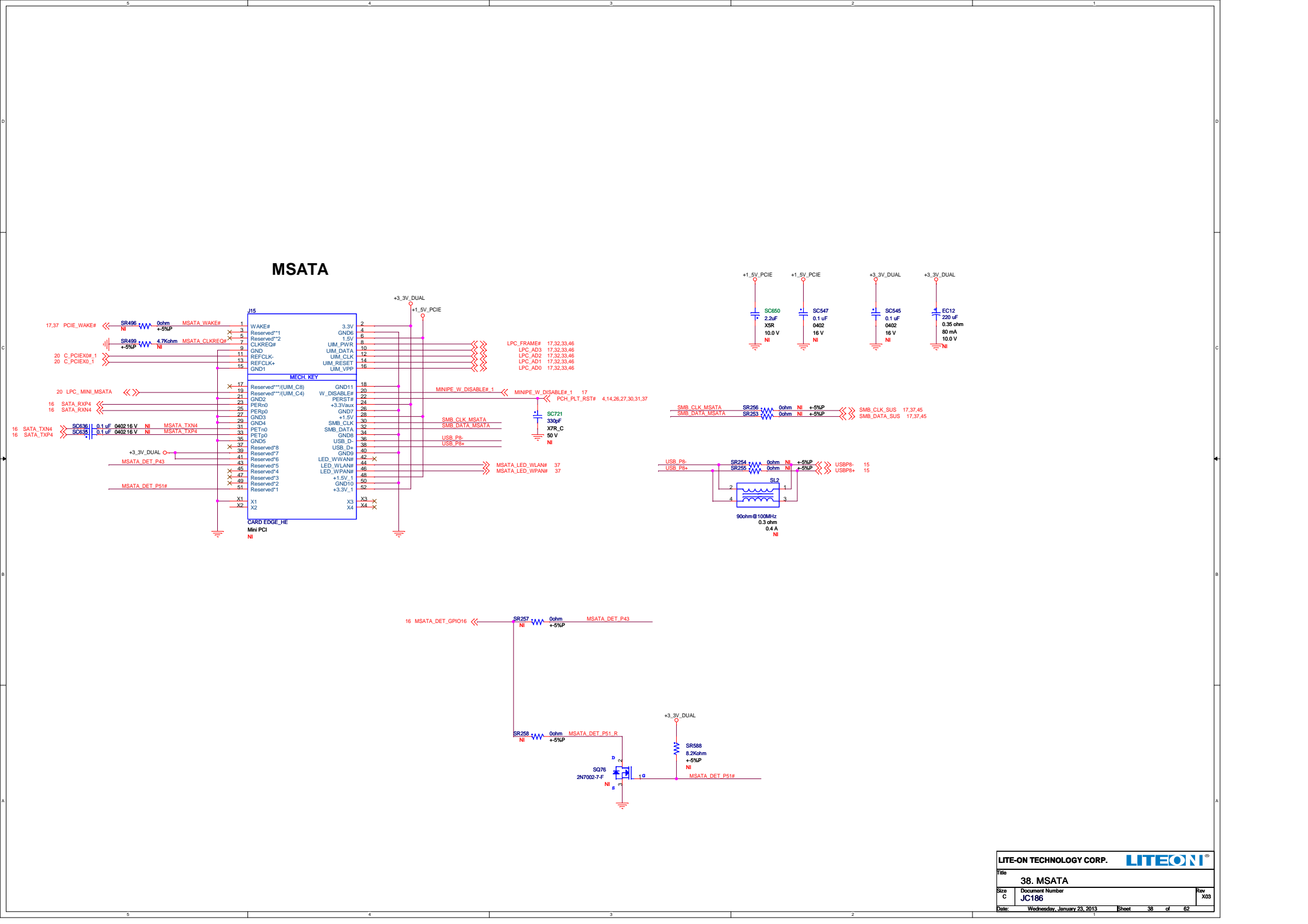
## Front Side USBx1



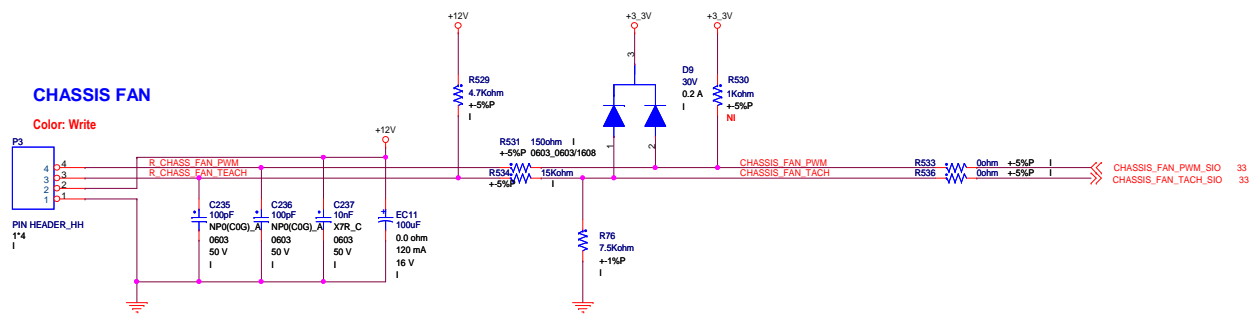
5V_DUAL_DISABLE#	H	H	L	L
SLP_S4#	H	L	H	L
+5V_USB_P4_EN	H	H	H	L

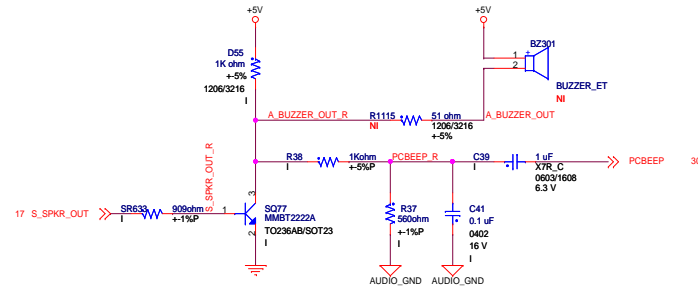
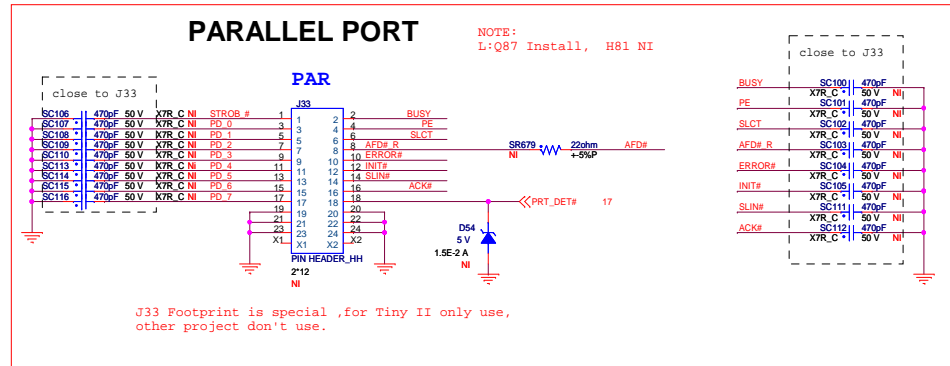
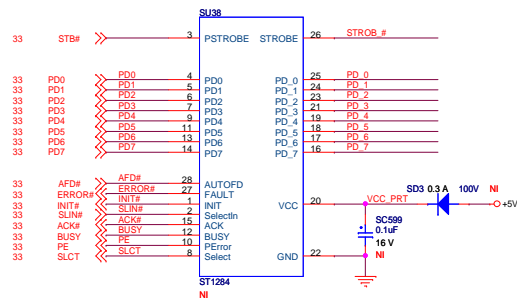




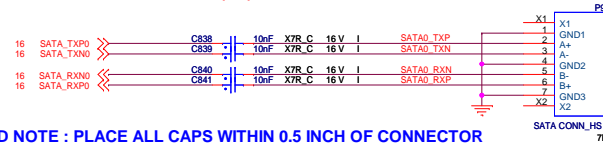
[illegible]

CHASSIS/CPU/PSU FAN

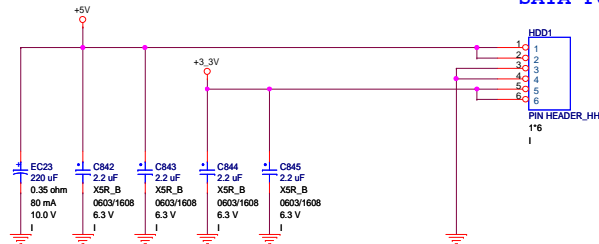


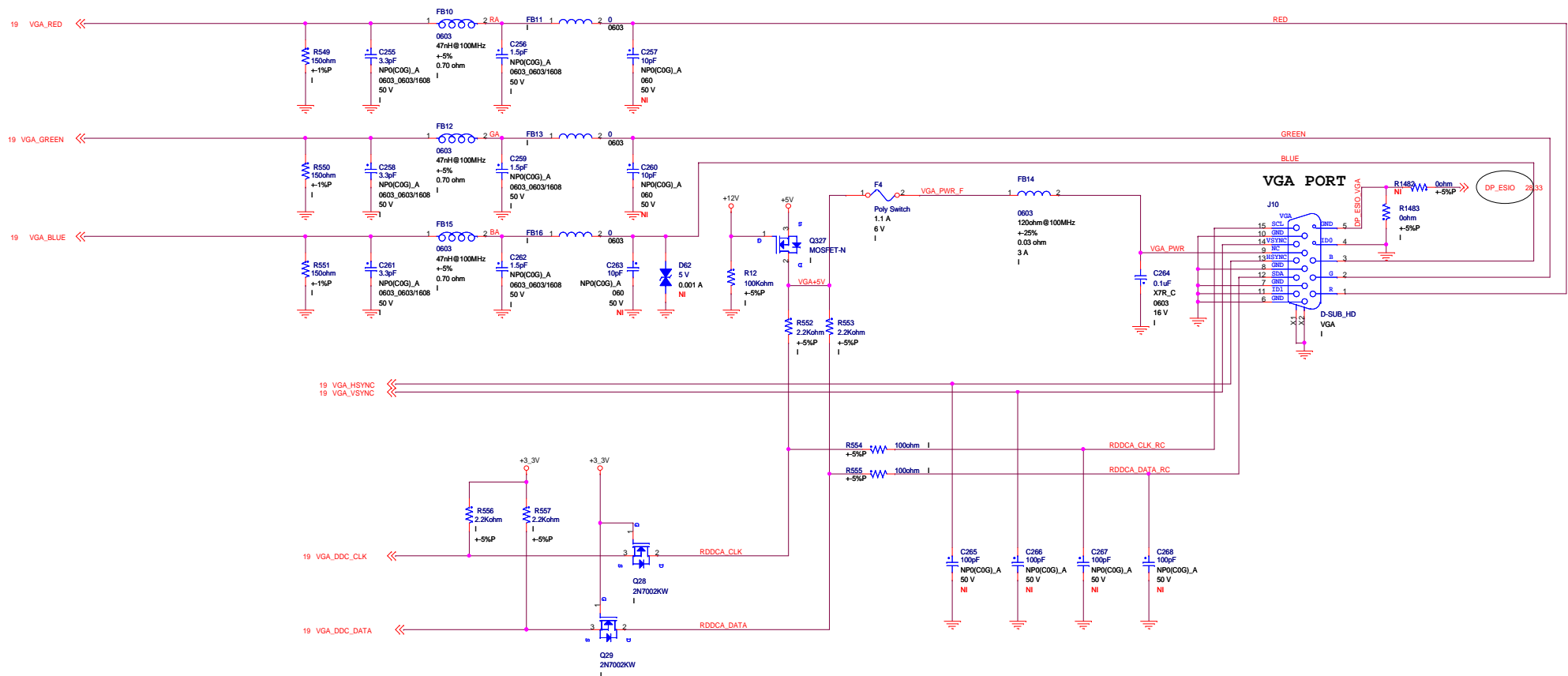
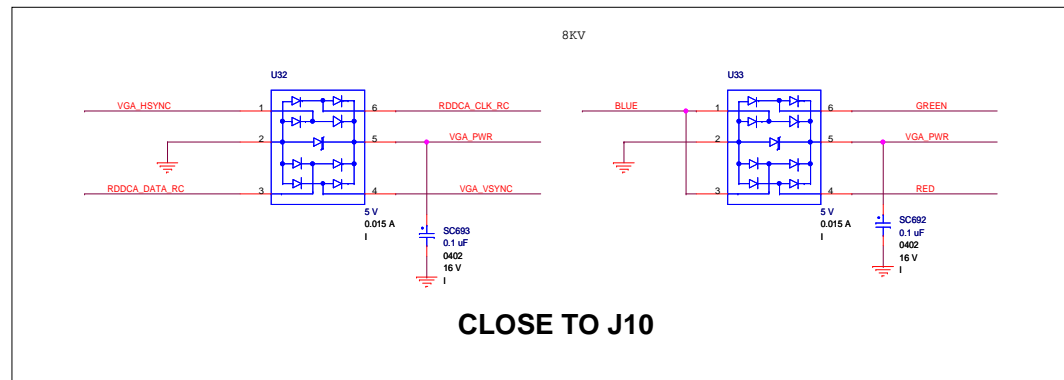


**CONTROLLER 1 SERIAL ATA 0 (3.0) - PRIMARY MASTER \_ DARK BLUE** **SATA SATA0**



**SATA Power**

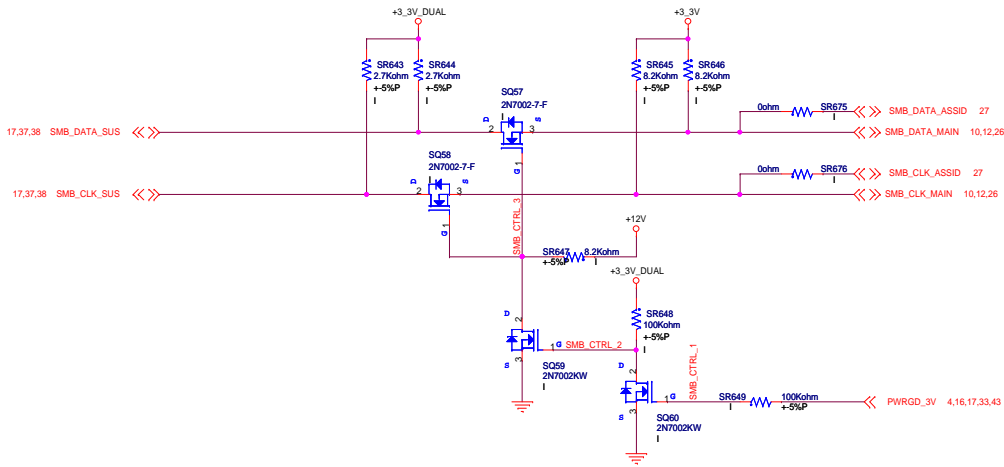




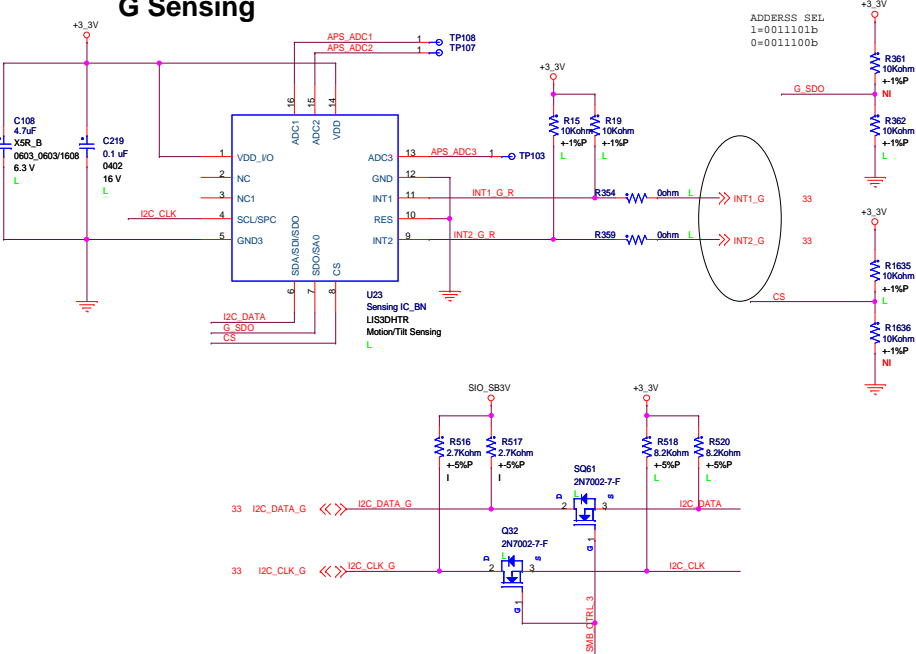




SM Bus

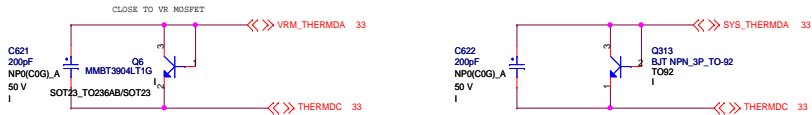


G Sensing



Temperature Sensing

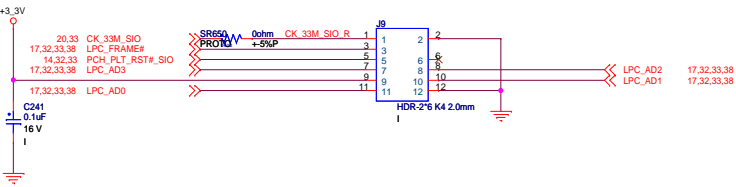
Current Mode



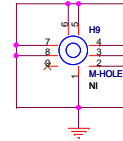
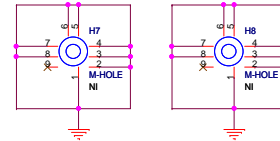
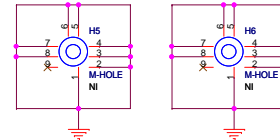
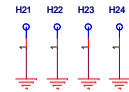
CAD NOTE : Place MLCC Close to Thermal Diode

Acceptable Transistor Component  
ST Micro: MMBT3904  
ON Semiconductor: MMBT3904LT1  
Fairchild Semiconductor: MMBT3904FSCT

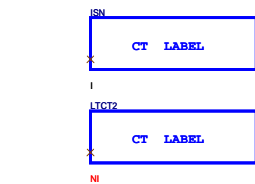
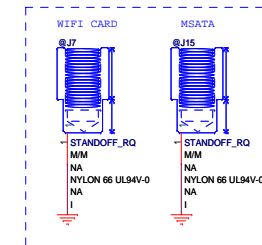
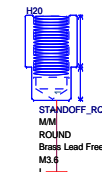
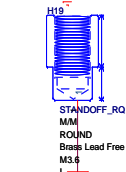
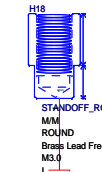
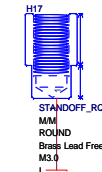
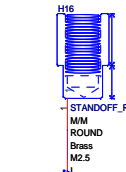
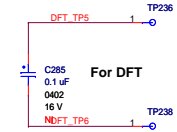
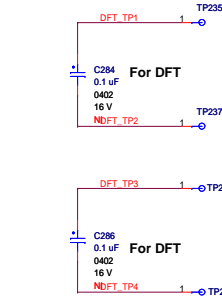
Debug port



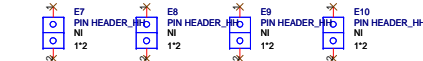
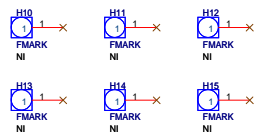
# CPU HEATSINK\_HOLE



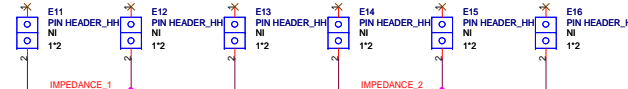
# FAN DUCT



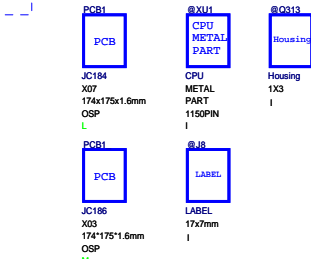
# For Impedance Test

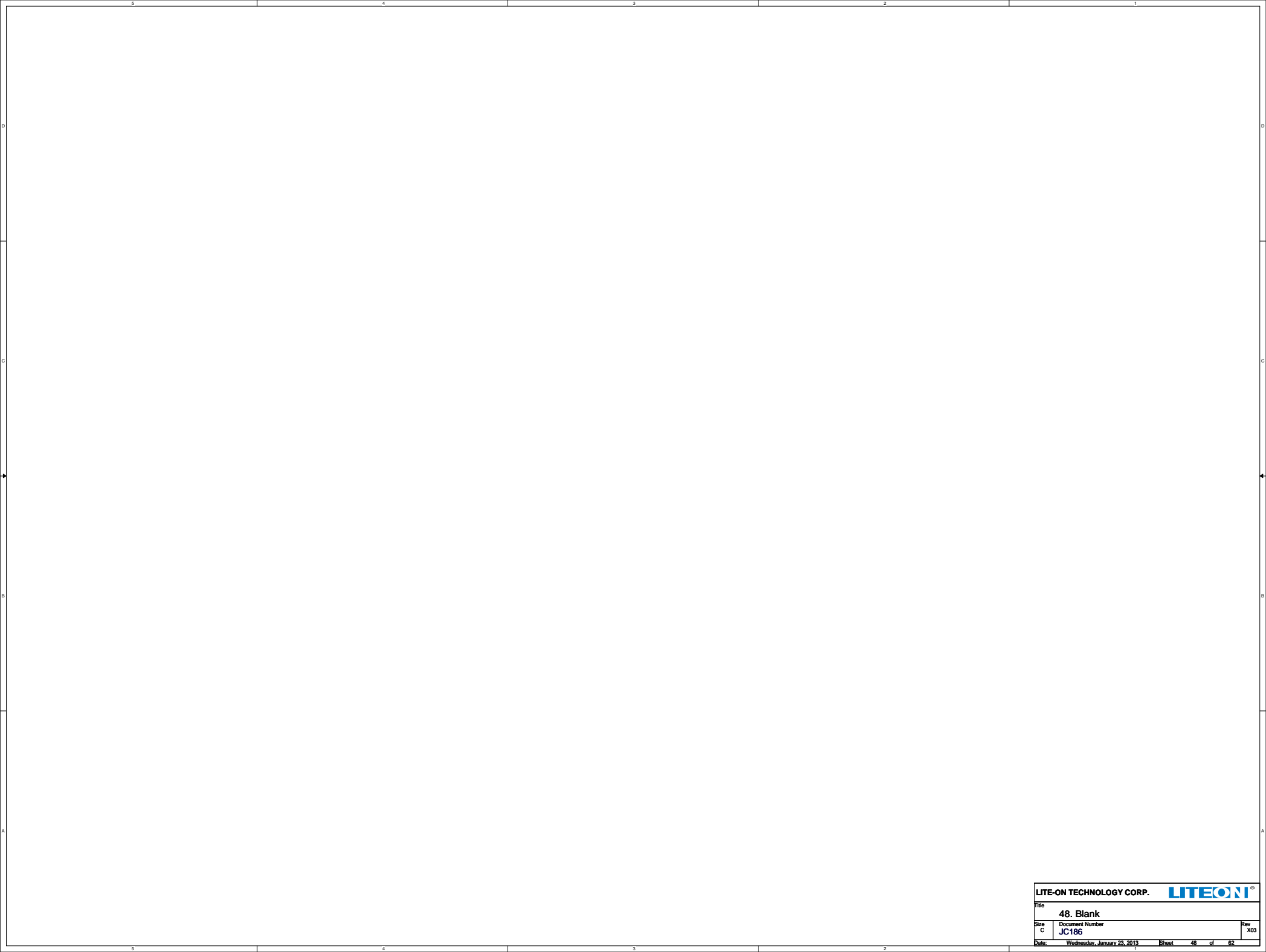



E7 differential 5/7 (85ohm) for USB2.0,USB3.0 for Layer1  
 E8 differential 4/5 (85ohm) for DMI , FDI ,SATA,USB for Layer4  
 E9 differential 6.5/4 (68ohm) for MEMORY for Layer4  
 E10 differential 4/10 (100ohm) for LAN for Layer6



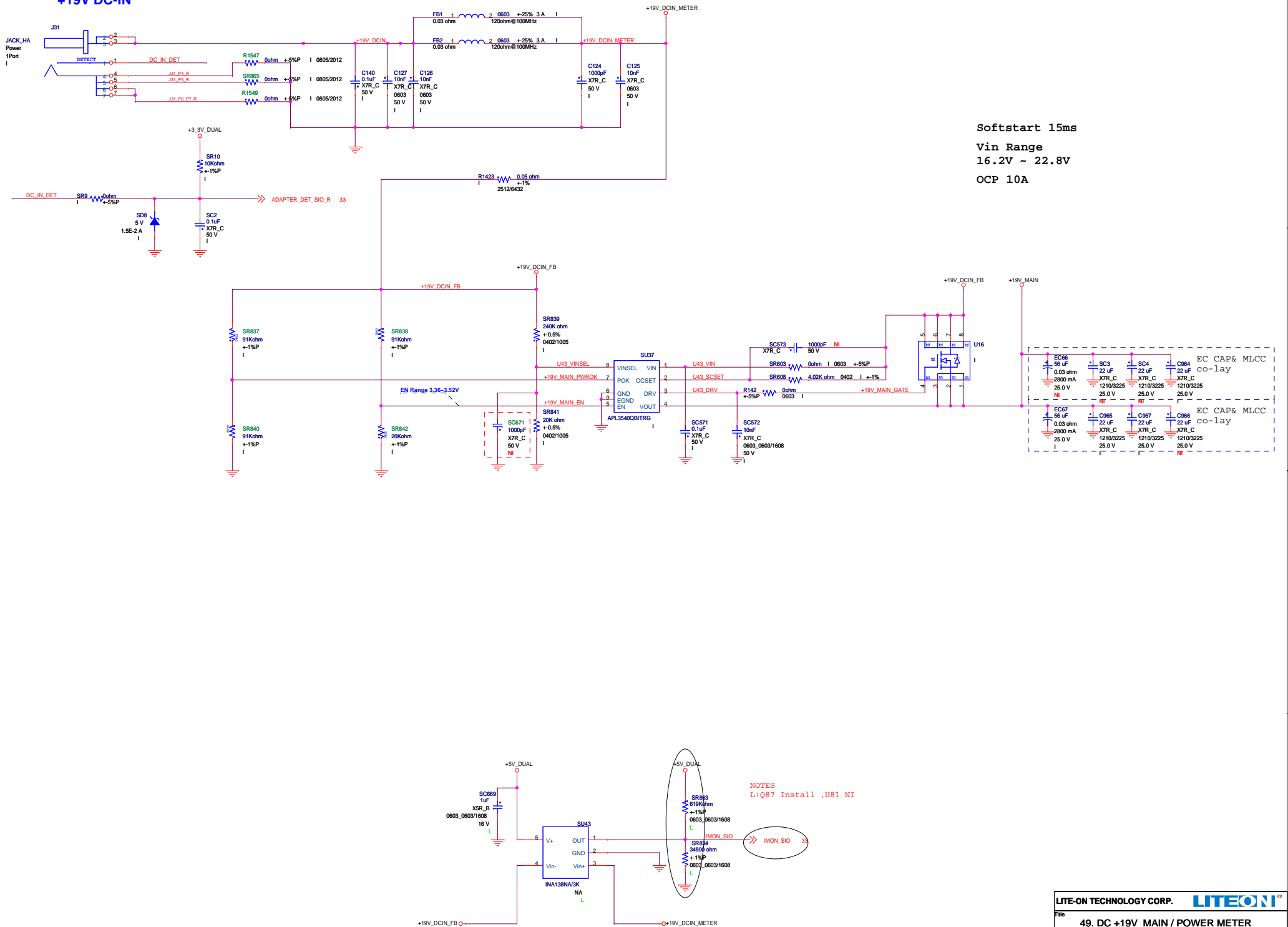
E11 single 4 for Layer 1  
 E12 single 4 for Layer 4  
 E13 single 9.5 (34ohm) for Layer 4  
 E14 single 6.5 (42ohm) for Layer 4





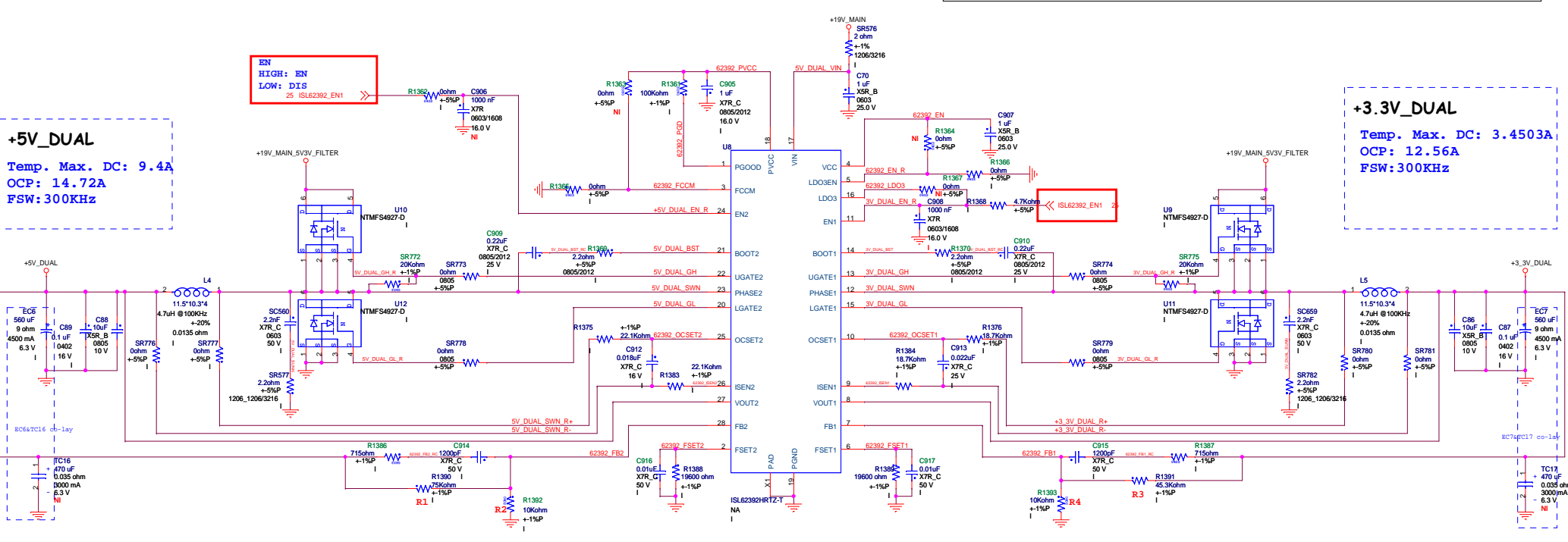
LITE-ON TECHNOLOGY CORP.			
Title			
48. Blank			
Size	Document Number	Rev	
C	JC186	X03	
Date:	Wednesday, January 23, 2013	Sheet	48 of 62

# +19V DC-IN



**+5V\_DUAL**  
Temp. Max. DC: 9.4A  
OCP: 14.72A  
FSW:300KHz

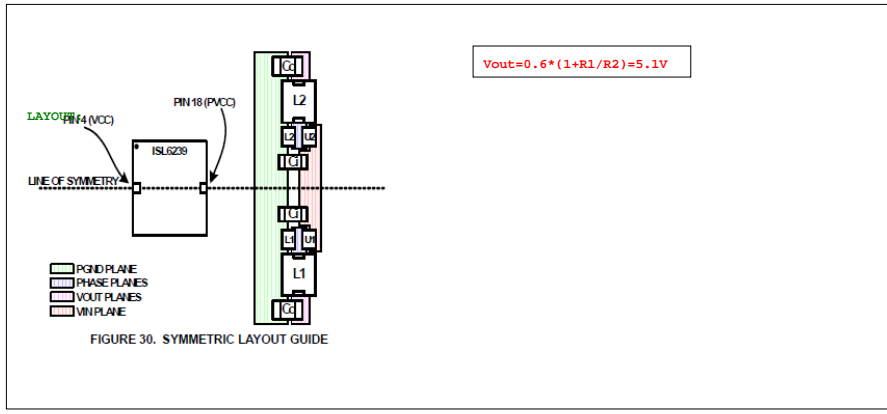
**+3.3V\_DUAL**  
Temp. Max. DC: 3.4503A  
OCP: 12.56A  
FSW:300KHz



$$V_{out} = 0.6 * (1 + R1/R2) = 5.1V$$

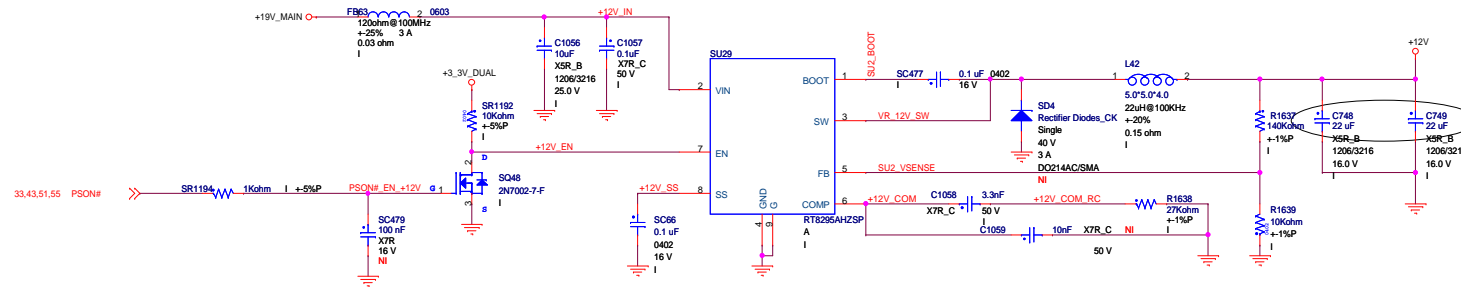
$$V_{out} = 0.6 * (1 + R3/R4) = 3.318V$$

FCCM	Level(Efficiency Mode)
<0.8V	Low(DCM enabled)
1.9V-2.1V	Float (audio filter enabled)
>2.4v	High(forced CCM)





# +12V



**+12V**  
 Temp. Max. DC: 0.7A  
 OCP: 4.3A

$$VO = VFB(1 + (R1/R2))$$

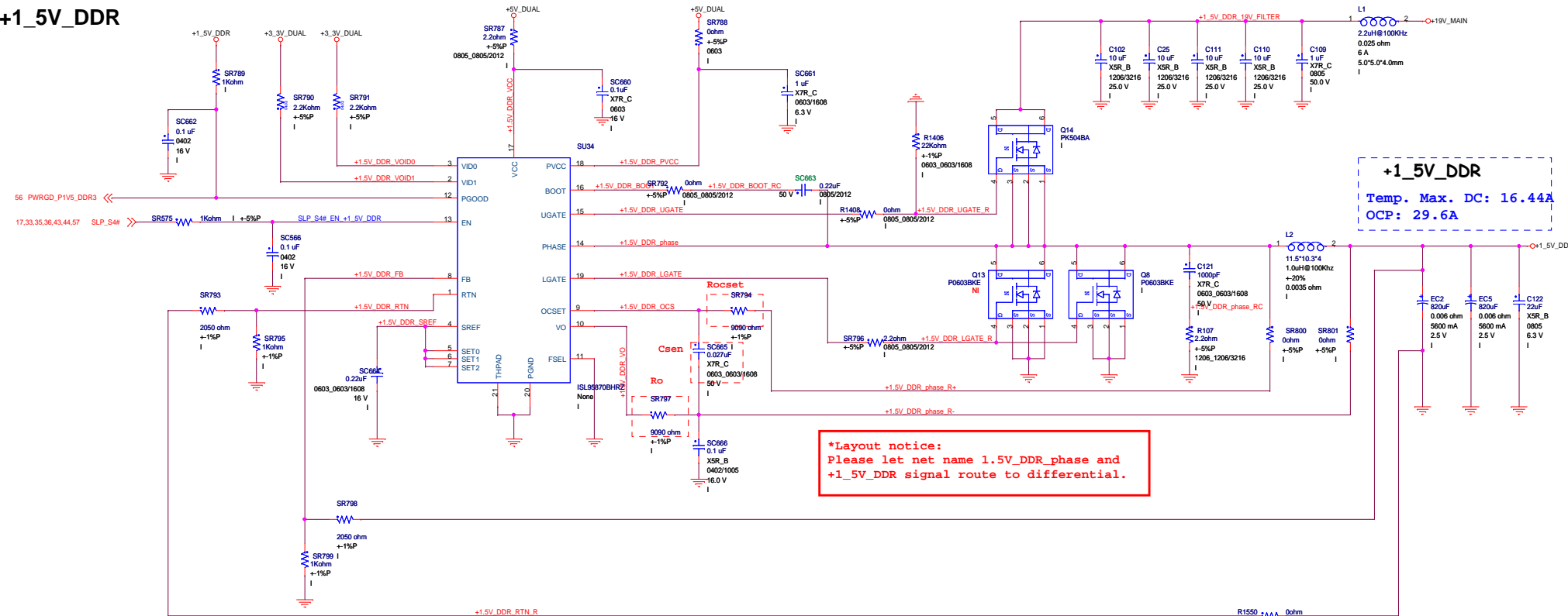
$$VFB = 0.8$$

$$VO = 12.05V$$





+1\_5V\_DDR



**OCP**

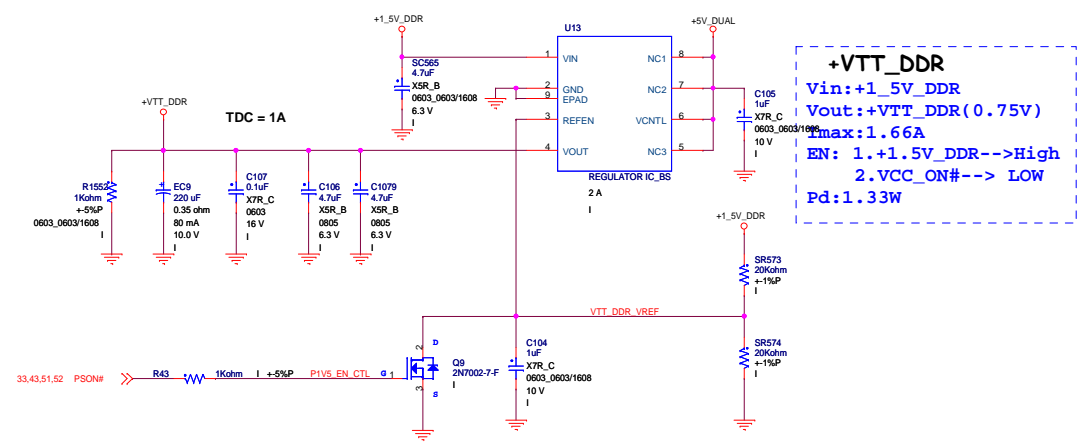
L=	1	uH
DCR=	3.5	m ohm
Ioc=	30	A
Csen=	27.21088	nF
Rocset=	10.5	K ohm
Ro=	10.5	K ohm

$R_{OCSET} = \frac{I_{OC} \cdot DCR}{I_{OCSET}}$

$C_{SEN} = \frac{L}{R_{OCSET} \cdot DCR}$

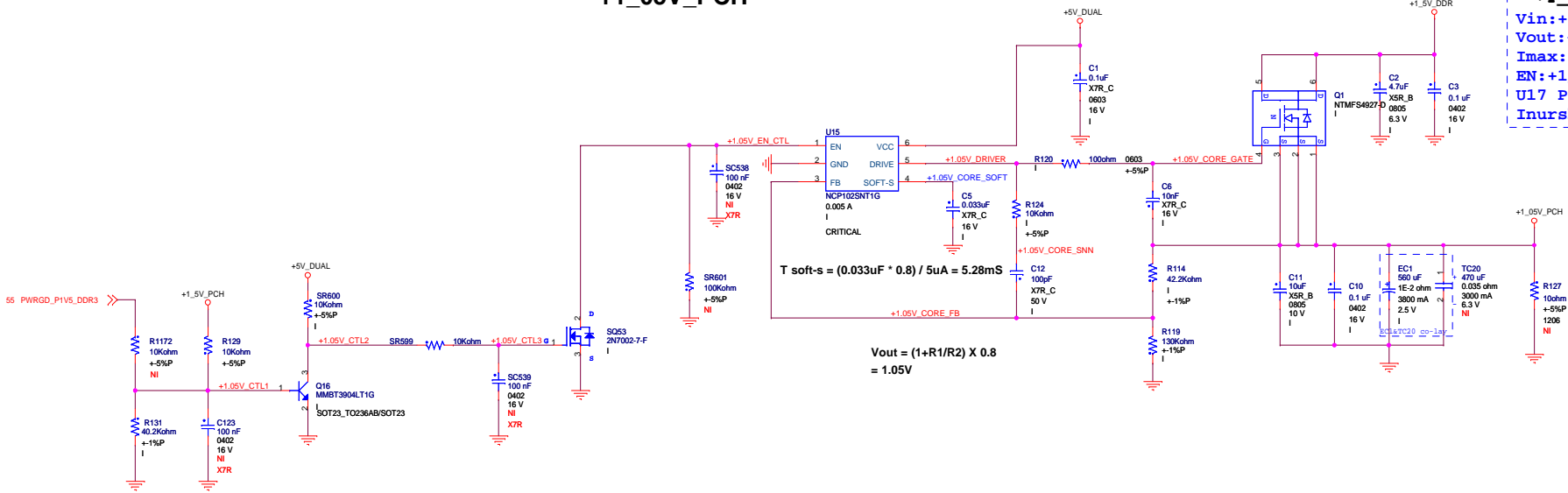
FSEL=>Pull this pin directly to GND for 300kHz.

check TINY SCH



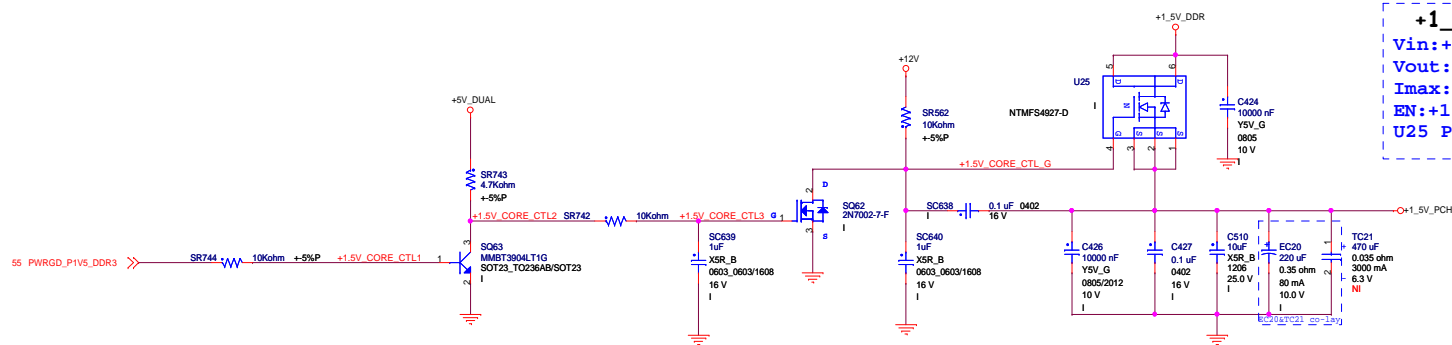
## +1\_05V\_PCH

**+1\_05V\_PCH**  
 Vin:+1\_5V\_DDR  
 Vout:+1\_05V\_PCH(1.05V)  
 Imax:5.295A  
 EN:+1\_5V\_CORE High  
 U17 Pd:2.7W  
 Inursh current:0.163A



## +1\_5V\_PCH

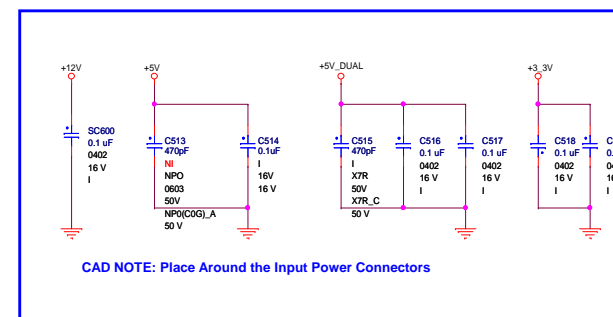
**+1\_5V\_PCH**  
 Vin:+1\_5V\_DDR  
 Vout:+1\_5V\_PCH(+1.5V)  
 Imax:0.183A  
 EN:+1\_5V\_CORE\_CTL\_G High  
 U25 Pd:2.7W



**+5V\_USB**

Close to each fuse

	SLP_S4#	VCCS_USB_EN	Q330/Q331/Q332
S0	1	1	ON
S3	1	1	ON
S4	0	0	OFF
S5	0	0	OFF



**+1\_05V\_ME**

$V_{out} = (1+R1/R2) \times 0.8 = 1.05V$

The schematic shows the internal components of the +1.05V\_ME regulator, including the U88 regulator IC, feedback network (R155, R146), output filter (C996, C995), and decoupling capacitors (C141, C143, C987, C402). The output voltage is calculated as  $V_{out} = (1+R1/R2) \times 0.8 = 1.05V$ .

$$V_{out} = (1 + R_1/R_2) \times 0.8$$
$$= 1.05V$$

+1\_05V\_ME

```
Vin:+3_3V_DUAL
Vout:+1_05V_ME (+1.05V)
Imax:0.67A
Pd:2W
```

The decoupling should be placed as close as possible to the processor power pins.

Signal	Usage	When Sampled	Comment
SPKR (S_SPKR_OUT)	No Reboot	Rising edge of PWROK	Set pull down. The signal has weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode
GPIO62 / SUSCLK (SUSCLK_GP62)	PLL On-Die Voltage Regulator Enable	Rising edge of RSMRST#	Set pull high. This has a weak internal pull-up Note: The internal pull-up is disabled after RSMRST#
GPIO55	Top-Block Swap Override	Rising edge of PWROK	Set pull high. The signal has weak internal pull-up . If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode
INTVRMEN (S_INTVRMEN)	Integrated V VRM Enable / Disable	Always	Set pull high. Integrated VRMS is enabled when INTVRMEN is sampled high
GPIO51	Boot BIOS Strap Bit[1] BBS[1]	Rising edge of PWROK	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-up.
GPIO19 / SATA1GP	Boot BIOS Strap Bit[0] BBS[0]	Rising edge of PWROK	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-up.
GPIO53	ESI Strap (Server/Workstation Only)	Rising edge of PWROK	Set pull high. This Signal has a weak internal pull-up.Tying this strap low configures DMI for ESI compatible operation.
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	Rising edge of PWROK	reserve pull up If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default) If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
GPIO36 (CLEAR_CMOS#)	RSVD	Rising edge of PWROK	Set pull high. This signal has a weak internal pull-down.
GPIO37 / SATA3GP (GPIO_37)	TLS Confidentiality	Rising edge of PWROK	Set pull high. This signal has a weak internal pull down. TLS CONFIDENTIALITY DISABLE LOW:DISABLE
DDPB_CTRLDATA (V_DDPB_CTRLCLK)	PORT B Detected	Rising edge of PWROK	When '1'- Port B is detected; When '0'- Port B is not detected. This signal has a weak internal pull-down.
DDPC_CTRLDATA (V_DDPC_CTRLDATA)	PORT C Detected	Rising edge of PWROK	When '1'- Port C is detected; When '0'- Port C is not detected. This signal has a weak internal pull-down.
DDPD_CTRLDATA (V_DDPD_CTRLDATA)	PORT D Detected	Rising edge of PWROK	When '1'- Port D is detected; When '0'- Port D is not detected. This signal has a weak internal pull-down.
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	Always	If strap is sampled high, the Integrated Deep Sx Well (DSW) On-Die VR mode is enabled.
GPIO36 / SATA2GP (CLEAR_CMOS#)	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal should not be pulled high when strap is sampled.
GPIO8 (IGE_EN#)	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull-up. NOTES: 1. The internal pull-up is disabled after RSMRST# deasserts. 2. This signal should not be pulled low when strap is sampled.



SIO IT8733F GPIO TABLE		
GPIO	Signal Name	Tiny II
GPIO_10(PIN84)	PCIRST3#/GP10	DP_ESIO (PU SB3V)
GPIO_11(PIN34)	PCIRST2#/GP11	+19V_VIN_CTL_SIO (PU SB3V)
GPIO_12(PIN33)	PCIRST1#/GP12	(NO USE)
GPIO_13(PIN32)	PWROK1/GP13	SIO_PWRGD_3V
GPIO_14(PIN31)	VCORE_ENPCH_C1/GP14	SMLINK1_CLK
GPIO_15(PIN3)	PCIRSTIN#/CIRTX2/GP15/CPU_PG	SIO_SCI2# (PU +3.3V)
GPIO_16(PIN2)	5VSB_CTLRL#/CIRRX2/GP16	SIO_SCI1# (PU +3.3V)
GPIO_17(PIN28)	RI2#/GP17	RI2-
GPIO_20(PIN27)	CTS2#/GP20	CTS2-
GPIO_21(PIN26)	DCD2#/GP21	DCD2-
GPIO_22(PIN25)	SCK/GP22	SIO_SCK
GPIO_23(PIN24)	SI/GP23	SIO_SI
GPIO_24(PIN23)	RTS2#/GP24	RTS2-
GPIO_25(PIN22)	DSR2#/GP25	DSR2-
GPIO_26(PIN21)	SOUT2/GP26	SOUT2-
GPIO_27(PIN20)	SIN2/GP27	SIN2-
GPIO_30(PIN19)	ATXPG/GP30	PWRGD_PS
GPIO_31(PIN18)	PWMOUT / GP31 / USBPWREN2#	SIO_CHR_USBPWREN (PU SB3V)
GPIO_32(PIN17)	DPWROK/GP32	SIO_GP32(NO USE)
GPIO_33(PIN16)	SUSACK#/GP33	SIO_PIN16_EC(4.7K PD)
GPIO_34(PIN15)	SUSWARN#/GP34	(NO USE)
GPIO_35(PIN14)	FAN_TAC4/GP35	INT1_G_SIO
GPIO_36(PIN13)	FAN_CTL3/GP36	INT2_G_SIO
GPIO_37(PIN12)	FAN_TAC3/GP37	SIO_PIN12(NO USE 4.7K PU)
GPIO_40(PIN79)	3VSB SW#/GP40	ME_CNTL
GPIO_41(PIN78)	PWROK2/GP41	SIO_SC#
GPIO_42(PIN76)	PSON#/GP42	SIO_PSON#
GPIO_43(PIN75)	PANSWH#/GP43	SIO_PB_IN
GPIO_44(PIN72)	PWRON#/GP44	PWRBTN_OUT#
GPIO_46(PIN66)	D_RX0/SMBCLK2/GP46/IRRX	SIO_RTCX2
GPIO_47(PIN65)	D_TX0/SMDAT2/GP47	SIO_RTCX1
GPIO_50(PIN48)	SO/GP50	SIO_SO
GPIO_51(PIN11)	FAN_CTL2/GP51	(NO USE)
GPIO_52(PIN10)	FAN_TAC2/GP52	SIO_PIN10(NO USE 4.7K PU)
GPIO_53(PIN77)	SUSC#/GP53	SLP_S4#
GPIO_54(PIN73)	PME#/GP54/USBPWREN1#	SIO_PME#
GPIO_55(PIN85)	RSMRST#/CIRRX1/GP55	RSMRST_N_SIO
GPIO_56(PIN83)	MCLK/GP56	2543_CLT1 (PU SB3V)
GPIO_57(PIN82)	MDAT/GP57	2543_EN (PU SB3V)
GPIO_60(PIN81)	KCLK/GP60	2543_CLT3 (PU SB3V)
GPIO_61(PIN80)	KDAT/GP61	CHARGER_OC_SIO# (PU SB3V)
GPIO_62(PIN45)	KRST#/GP62	KBRST#
GPIO_63(PIN6)	SLP_SUS#/VLDT_EN/GP63	5V_DUAL_DISABLE#
GPIO_70(PIN113)	KSI0/GP70/PD0	PD0
GPIO_71(PIN114)	KSI1/GP71/PD1	PD1
GPIO_72(PIN115)	JP1/KSO0/GP72/PD2	PD2
GPIO_73(PIN116)	KSO1/GP73/PD3	PD3
GPIO_74(PIN117)	KSO2/GP74/PD4	PD4
GPIO_75(PIN118)	KSO3/GP75/PD5	PD5
GPIO_76(PIN119)	KSO4/GP76/PD6	PD6
GPIO_77(PIN120)	KSO5/GP77/PD7	PD7
GPIO_85(PIN64)	IO_SC#/GP85/SMBDAT0	APS_I2C_DATA
GPIO_86(PIN63)	GP86/SMBCLK0	APS_I2C_CLK



**X06 12042012**  
(1) Page 43&P51 , add SR1277,SR1278,SQ85 for VccCore have No-Monotonic after power down at S0 to S5 mode  
(2) Page 33 , add SC753 for IMON\_SIO  
(3) Page 49 , add (co-lay) C962,C963,C964,C965,C966,C967, change EC66,EC67 to DIP type for +19V\_MAIN  
(4) Page 17 , modify ME\_disable sch (add R1678)

**X06 12052012**  
(1) Page 50/54/55 , change C864,C865,C919,C920,C873,C874,C921,C945,C102,C25,C110,C111 C48,C49,SC553,C52,SC562,SC668,C53 vendor for CPU noise  
(2) Page 29 , add R1679 0ohm to NI for redriver sch

**X06 12062012**  
(1) Page 55 , change SR795 to 1K ohm for +1\_5V\_DDR  
(2) Page 26 , change SR626,SR629 to I,@J21(1-3)1,@J20(1-3)1, J21,J20 to NI for SPI ROM SCH.  
(3) Page 29 , change SC593,SC594,SC626,SC701,SC702,SC703,SC704,SC705,SC706,SC707,SC708, SC709,SC710,SC712,SC713,SC714,SR19,SR20,SR21,SR22,SR30,SR34,SR35,SR36,SR67,SR68,SR70, SU2,C962,C963,Q118,R20,R21 to C30,C31,C32,C33,C34,C35,C36,C37,C38,C61,C62,C63,C64,C65, C66,C67,R45,R46,R47,R48,R49,R50,R51,R52,R53,R54,R55,U1,SC3,SC4,SQ1,SR1,SR2 (Redriver IC from bottom side move to top side)  
(4) Page 26&P31 , change C56 to 15pF for Y1 32.768k crystal (PCH), SC462 to 27pF for SY1 25MHz crystal (LAN)

**X06 12072012**  
(1) Page 30 , change R1677 to I, R1676 to NI for audio noise(G3 mode)

**X07 12172012**  
(1) Page 18 , change netname, from PCH\_GP71\_PU change to BRD\_ID5  
(2) Page 40 , change SQ77 vendor, from DII change to PANJIT

**X07 12242012**  
(1) Page 49 , SC573 change to NI,SC572 change to 10nF for 19V\_MAIN OCP issue with Battery BOX.  
(2) Page 53 , R1314 change to 7.5Kohm for L7 thermal protection point.  
(3) Page 30&47 , add R1680 0ohm for Digital GNDand analog GND,add R1681 0ohm for FAN DUCT to GND.

**X07 12262012**  
(1) Page 32 , SU9 change symbol to ST33ZP24AR28PVSP (TPM)  
(2) Page 55 , Q8,Q14 change Vender to NIKO

**X07 01022013**  
(1) Page 31 , change Foxconn RJ45 connect to JFM3811B-2104-4F (Return Loss)  
(2) Page 36 , change USB charger IC to TP2546  
(3) Page 30/42/45 , change Q28,Q29,Q31,SQ59,SQ60 to 2N7002KW  
(4) Page 24 , change @E1(1-2) to H=6mm  
(5) Page 25 , add PCH\_RSMRST# Pull down SCH.

**X07 01082013**  
(1) Page 14~21,23 change PCH U2 sysmbol to DH82Q87 QE8X  
(2) Page 31 , change SU10 LAN IC symbol to WGI217LM QQ4R

**X07 01102013**  
(1) Page 40, change SC106,SC107,SC108,SC109,SC110,SC113,SC114,SC115,SC116 to NI for PARALLEL PORT  
(2) Page 42 , change C256,C259,,C262 to 1.5pF,D62 to NI for VGA

**X07 01112013**  
(1) Page 25, add SUSWARN# to SUSACT# Delay Circuit, R1036, R1034, R1038, R1041, R1044, R1048, C639, Q116, Q119, Q120 change to Stuff, R1047 change to 1M, add C682 1uF  
(2) Page 17 , change R1560 to NI, for SUSWARN#, SUSACT# delay circuit  
(3) Page 24 , change SR51 from 20K ohm to 22.1K ohm for RTCRST# delay

**X07 01122013**  
(1) Page 26 , change SR352 from 249 ohm to 1K ohm for CRB check  
Page 4, Change R1621 from 1K to 10K ohm for CRB check

**X07 01152013**  
(1) Page 56 , change SR601 to NI for +1.05V\_EN\_CTL

**X07 01162013**  
(1) Page 26 , change @U6,@XU6 SPI ROM for support Quad IO

**X07 01182013**  
(1) Page 30&40 , change R1115,BZ301,D61 to NI, change D55 to 1K ohm,R37 to 560 ohm,R38 to 1Kohm for Buzzer Circuit  
(2) Page 38 , change MASTA Circuit to NI.  
(3) Page 37 , change SU31,SC489,SC491,SR1202,SR1203,SC334,SC490,SC492,C781,C782,C783,C784,C785,C786,C787,C788 to NI for 2 COM change to 1 COM.  
(4) Page 40 , change SU38,SC599,SD3,J33,SR679,D54,SC100,SC101,SC102,SC103,SC104,SC105,SC111,SC112 to NI, for LPT Circuit

**X07 01212013**  
(1) Page 04 , change R1273 to 3.24K for VCCST\_PWRGD

**X07 01222013**  
(1) Page 53 , change R1309 to 124k ohm for IMON